The status, needs and potential solutions related to *testing photonic devices and products* that Incorporate Photonic Integrated Circuits (PIC)

IPSR Webinar
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Thomas G. Brown, The Institute of Optics, Univ. Rochester

Richard Otte, Promex Industries

With contributions from

Dave Armstrong, Keren Bergman, Stefan Preble

Link to recording (good for six months after the webinar): http://bit.ly/2m0iodm

Outline

- Acknowledgments
- The Status of Optical Electronics and Testing
  - With a **Photonic Integrated Circuit (PIC) emphasis**
- What Is to Be Tested
- Optical Electronic Product Testing
  - Generic Test Needs
  - Optical Test vs Electronic Test
  - Optical Test Ports
  - Test Cost
  - Optical Test Issues
- Roadmap Results
  - Test Challenges, Barriers, Unfilled Needs, Potential Solutions, Test Gaps & Show Stoppers
- Testing at AIM-Photonics

Text Color Code Key
Blue Key Point
Red is a Barrier
Green is a Cost Issue

Acknowledgments

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- Dave Armstrong, Advantest, AIM-IPSR Roadmap Test TWG Chair
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- Chris Coleman, Keysight

Other individuals in addition to those listed above contributed content incorporated in this presentation. Many contributed via the MIT CTR workshops and other interactions.

AIM Team:
Keren Bergman, Robert Polster, Columbia Univ.
Stefan Preble, Donald Figer, RIT
Ed White, Tom Miller, Anthony Lisi, SUNY Poly
Thomas Brown, Ben Miller, Jaime Cardenas, University of Rochester
Alan Evans, Corning
Justin Bickford, DoD (ARL)

The Status of Optical Electronics and Testing

With a Photonic Integrated Circuit (PIC) Emphasis

Photonics Industry and related technology

- ~$8 Billion of Data Transmission Revenue; Telecom, Data Centers, etc.
  - Much Single Mode (SM). Telecom is the oldest, most Developed application
  - Data Centers are growing, utilize Active Optical Cables (AOCs) for >1 meter.
  - Optics on circuit board being Explored
- Photonic Integrated Circuit Types, primarily SM
  1. **InP & Si CMOS: optical and electronic**
  2. **Si: Only passive optical with hybrid for active**
  3. **Glass: passive optical and electronic with some hybrid for actives**
- **Typical Technology**
  - **CMOS transistor bandwidth max of ~50 GHz limits max data rate/lane**
    - **Multiplexing of lanes is common**
      - Polarization
      - Quadrature & higher order modulation (e.g. DP NQAM)
      - Wavelength
      - Multiple fibers
  - Wavelengths are ~650nm to ~1700 nm; **(datacom > 1 micron, typically 1.3-1.6 µm)**
  - Datacom: 10 dBm laser power; 1A/W detector sensitivity, 20 dB optical budget

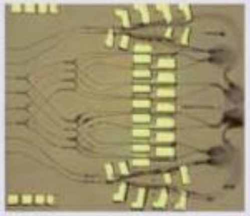
Market Trends & Forecasts

- Demand for more data transmission & processing is growing exponentially driving optical DataCom
  - **Multiple Companies NOW introducing 400Gb/s DataCom products.**
  - **Infinera is shipping products today using InP with 500+ photonic devices/die.**
- Much Interest in utilizing Single Mode (SM) optical technology PICs for more than Datacom
  - Sensors, Etc.
- **Multi Mode (MM) widely used in sensors and DataCom.**
  - **Automotive for Low cost with plastic fiber, push-on connectors**
  - **Minimal implementation of MM with PICs**

Photonic Devices/Products to Be Tested

Prototypes across market sectors

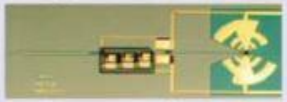
Optical switching



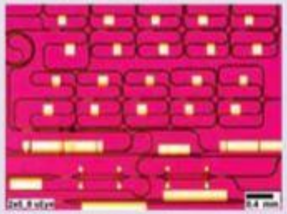
4x4 space and wavelength selective switch

Fast optical switch matrix

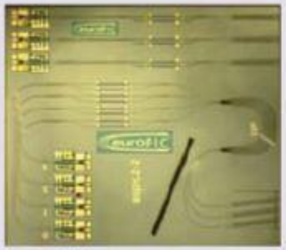
THz Optical to RF converter



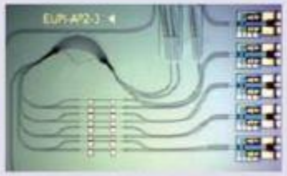
Fiber sensor readout



Brillouin strain sensor readout

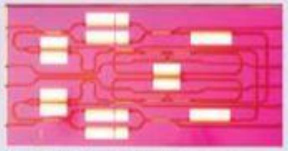


Fiber Bragg Grating readout



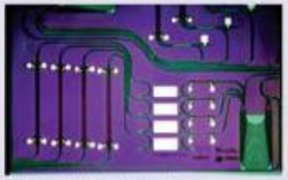
Fiber Bragg Grating readout

Variety of lasers



Widely tunable ring laser

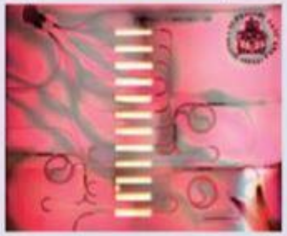
Variable repetition rate pulse laser



Filtered-feedback multi-wavelength laser

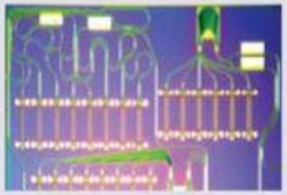
tunable laser with integrated MZI modulator

Optical data handling



All-optical regenerator for constant envelope WDM signals

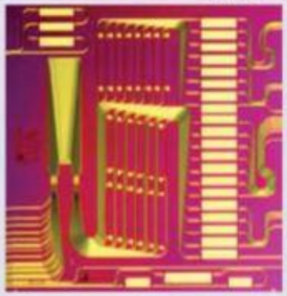
WDM to TDM Trans-Multiplexer



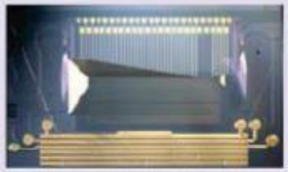
Pulse serialiser

GPSK receiver

Medical and bio-imaging

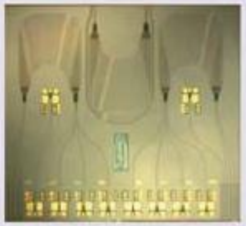


Pulse shaper for bio-imaging



Integrated tunable laser for optical coherence tomography

Fiber to the home

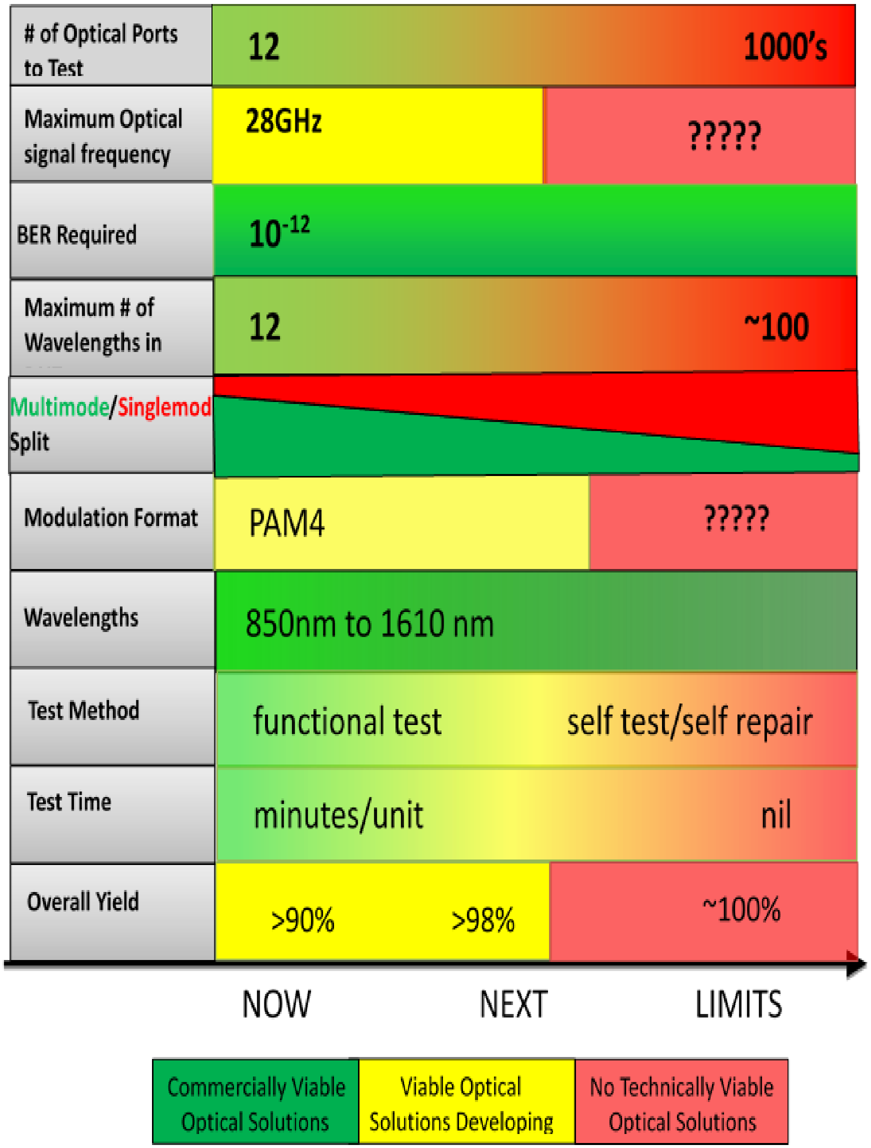


WDM receiver

PhotonDelta
Integrated Photonics Ecosystem

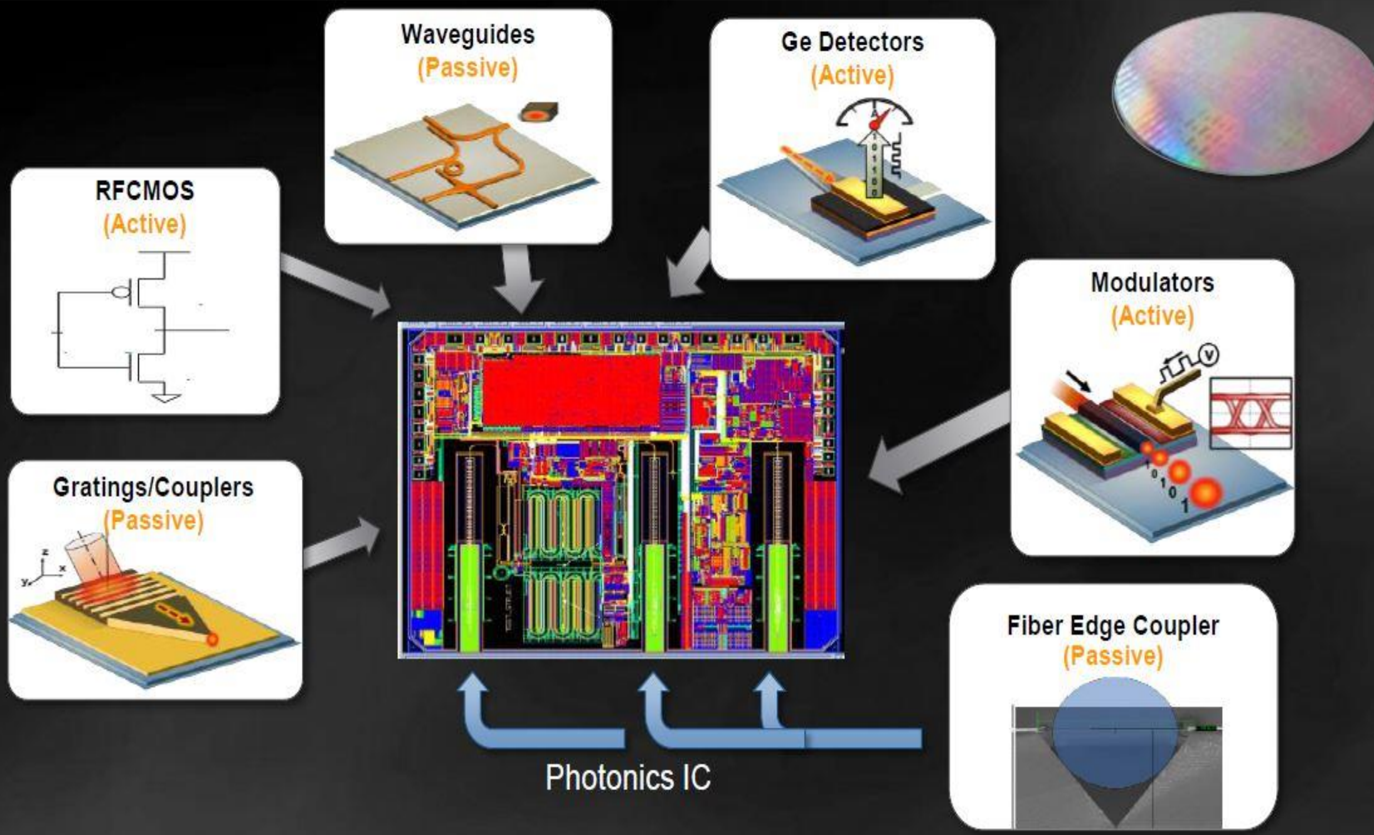
Next phase is enabling the supply chain

Datacom Key Test Attributes



From IPSR Test Chapter

Silicon Photonics Foundry Platform



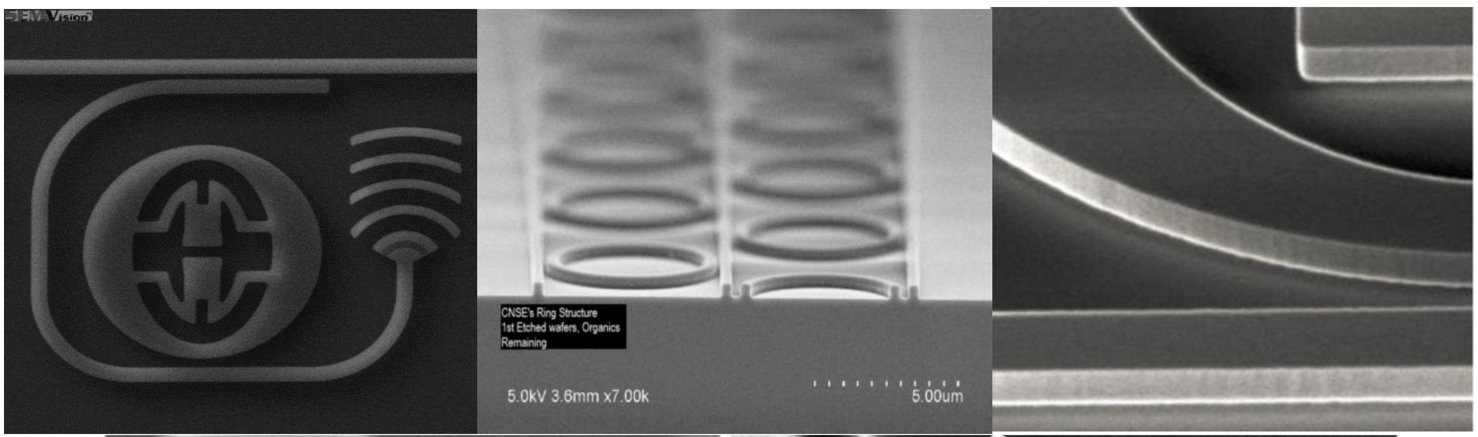
All function except light source integrated into Si foundry flow

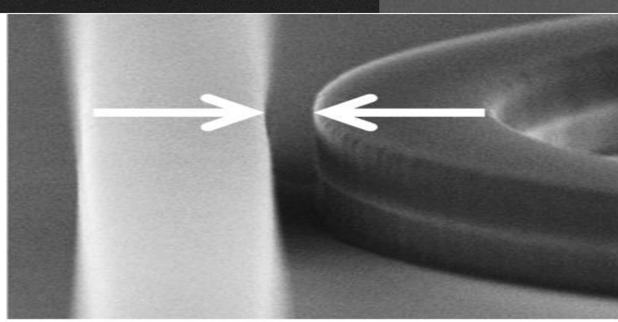
Question of Silicon Photonics fit into Si foundry: ***Demonstrated***

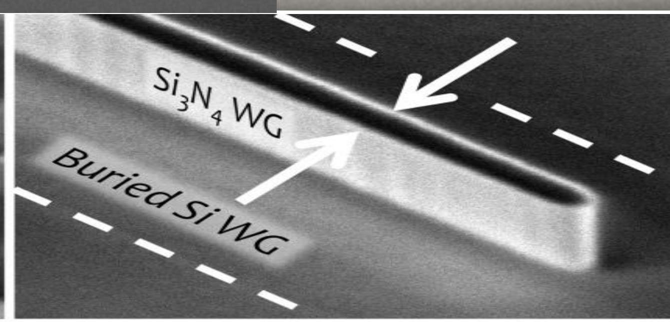
*Graphics: GF, IBM, IME

AIM Photonics Foundry Processes

- MPWA for silicon photonics structures at SUNY Poly
  - Advanced lithography and etch for low loss photonics devices
  - Waveguides, high-speed modulators, filters, gratings, Ge detectors
  - Verified PDK library for both devices and interconnections

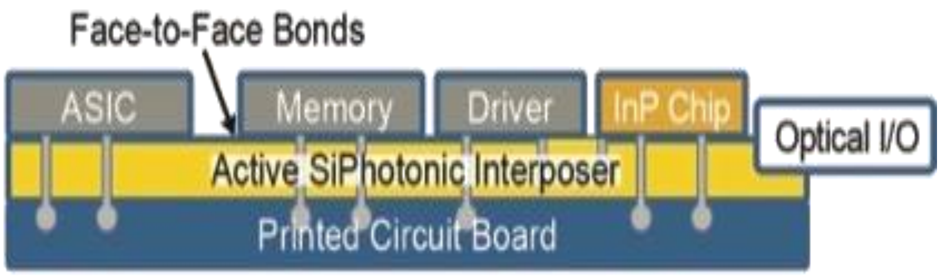



95nm gap in Si.



95nm Si3N4 taper on Si waveguide.

The Photonic Interposer



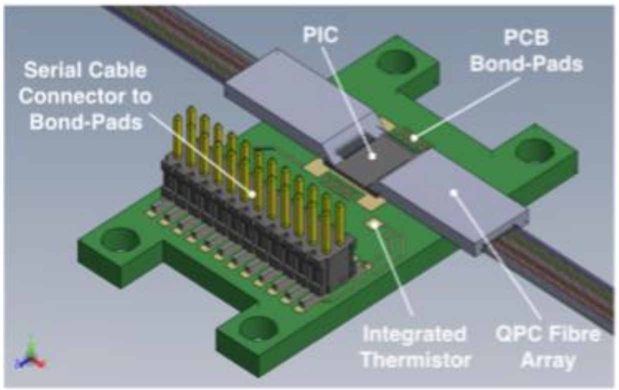
- An Emerging Key Component
- An interposer is similar to a small, thin circuit board with different technology die mounted on it.
  - Provides electronic and photonic connections between devices
  - Increases IO pitch to enable connections to PCB, usually with a bump array
  - Often provides an interconnection for the optical signal/s or laser light source/s
- Interposers can be made of silicon or glass, not organics
- Photonic interposers require waveguides:
  - Silicon Nitride (passive) or SOI (active)
  - ~1 micron wide
  - < 1 micron alignment accuracy required

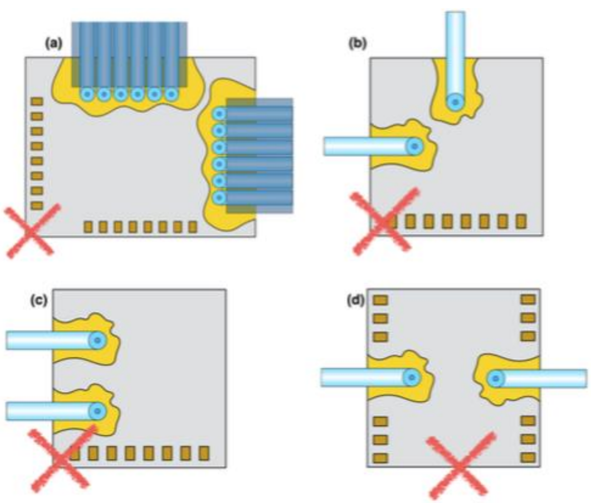
Optical I/O

- Needed for both test and operation
  - Where does the light come from?
  - How is it sensed during the testing process?
- Grating couplers (Good for accessing device layer before singulation)
  - In functional I/O (high efficiency needed)
  - Essential for wafer level testing.
  - Low spectral range, polarization sensitivity.
- Edge couplers
  - High spectral range, potentially low polarization sensitivity.
  - Hard for wafer level testing.
- Application dependent considerations
  - Datacom: Eventual need for dense fiber arrays.
  - Sensors: Eventual need for on-board sources (no fibers).

Tyndall Institute (Cork, Ireland) packaging

February 2016
Concentrates on Optical I/O
Summary sections on
- Thermal management
- Standard PIC-to-PCB





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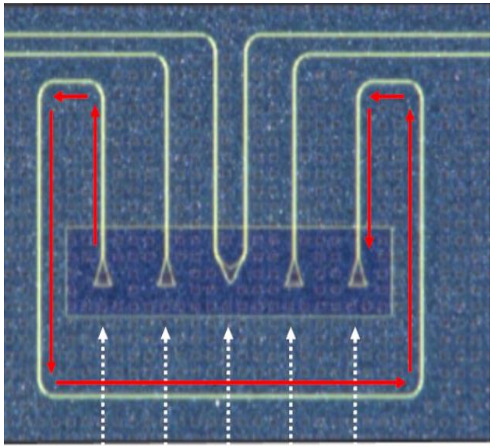
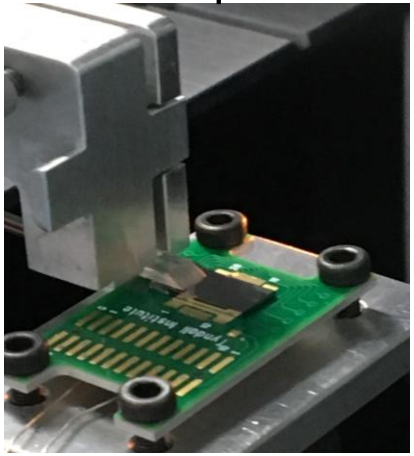
Tyndall fiber array packaging

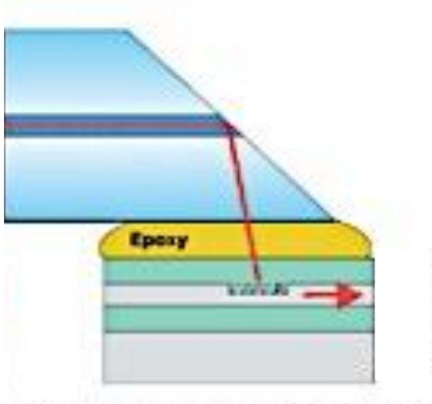
- Auto aligner manufactured by Newport
- Row of grating couplers (10° coupling) with optical shunt on ends to aid in alignment.
- Rough alignment performed manually and optimized by auto align system
- Planar and vertical coupling

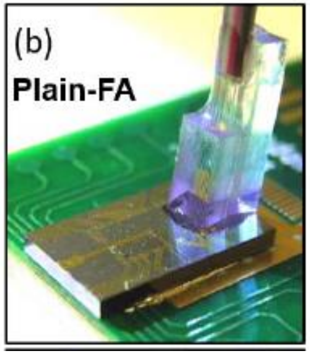


Carroll et. al, *Appl. Sci*, **6**, 462 (2016)

Planar coupler

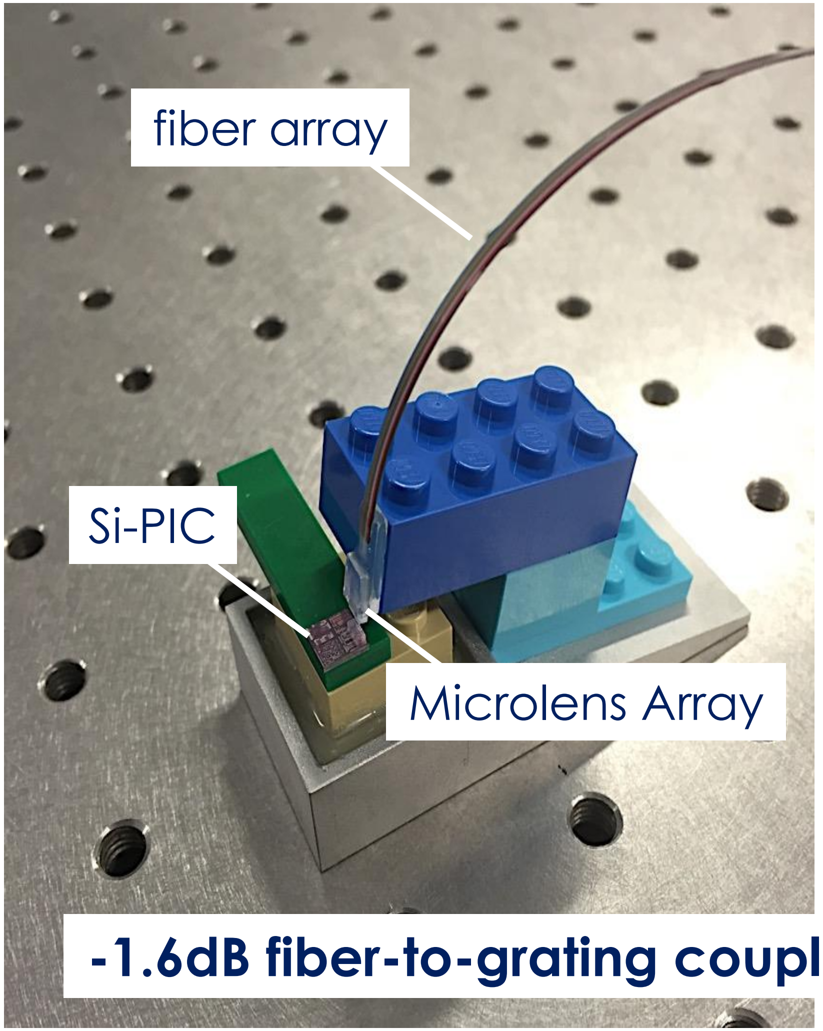






Vertical coupler

Tyndall: Pluggable connector



-1.6dB fiber-to-grating coupler

Active vs. Passive Fiber Attach

Active Alignment Requires
- An external source (part of the test setup)
- Method of sensing coupled power
  - TAP + Detector (single fiber or fiber array)
  - Loop back (for fiber arrays)

Passive Alignment Requires
- Structures to Constrain Fiber Positioning
  - U-groove (AIM Interposer)
  - V-groove (under evaluation)
  - Prefabricated fiber array with alignment marks

Designed for Passive Alignment

- Single interposer that can be used for various silicon photonic IC's and systems for prototyping

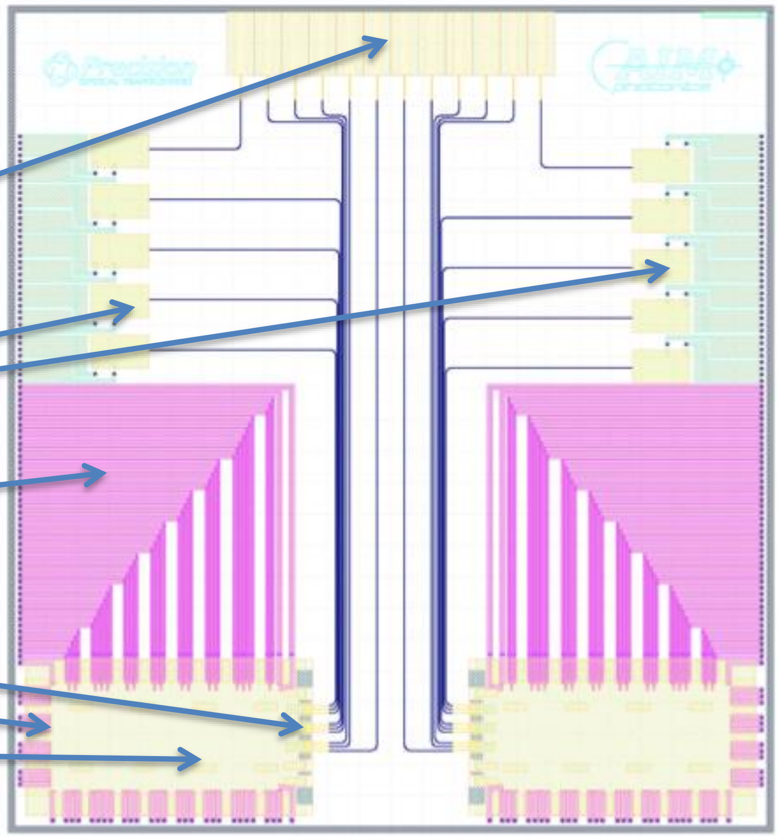
Passive SiN waveguide technology

Fibers in trenches for passive alignment

Eight laser slots

Standard Electrical and Optical I/O on PIC

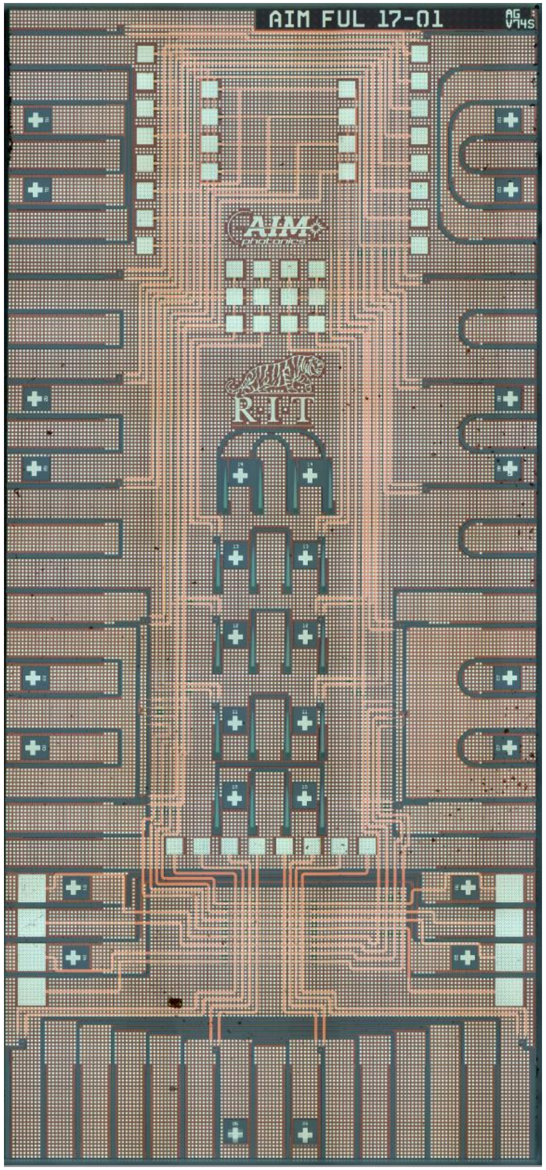
Two PIC slots
(mirror image layout)



Actively Aligned Fiber Attach

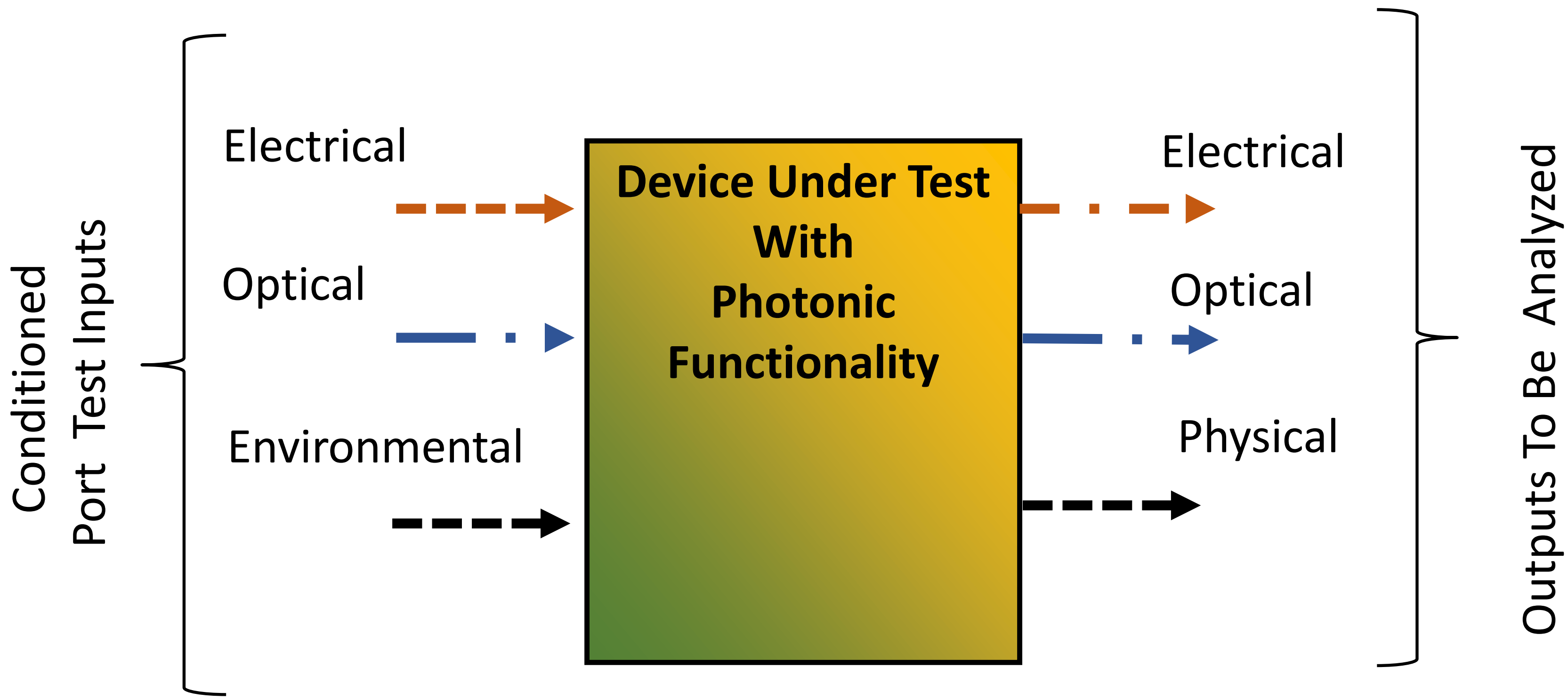
Loopbacks for actively aligned fiber attachment (4, 8 and 16 fiber designs)

- Non-local and local (nearest neighbor) alignment strategies
  - On/off chip (photonic only)
  - Photodetector
  - 1% Tap to Photodetector
- Edge coupling
  - Silicon nitride (right side)
  - Silicon (left side of chip)
- Grating coupling to Silicon or SiN in center



Photonic Product Test

Generic Photonic Product Test Environment



Life Cycle Flow

Stage of Life Cycle / **Typical Optical Tests**

Design & Development
To Evaluate Various Designs

- As Determined by Engineering. Typically:
  - HAST
  - Margin Checks
  - Temperature Dependence
  - Component Tolerance Impact

Qualification
To Ensure the Product Meets Requirements

- Environmental Extremes OK
- Power/Voltage Variation Impact OK
- Bit Error Rate OK
- Input Signal Extremes
- Output Signal Extremes
- Attenuation, Signal-to-Noise, Jitter, Skew OK
- Evaluate Multiple Lots
- Temperature Rise
- Mechanical Dimensions
- Perform Over Temperature Range
- Extrapolated Performance Meets Specifications

Validation
To Ensure the Manufacturing Process Produces Consistent Quality

- Output Signal Quality
- Power consumed
- Temperature Rise
- Dimensions To Spec
- Acceptable Eye Diagram, & Yield
- Evaluate Lot-to-lot Variation

Production
To Monitor Ongoing Quality

- Measure Key Parameters, often sampling:
- Output Signal Quality
- Power consumed
- Temperature Rise
- Dimensions to Spec
- Acceptable Eye Diagram

In Use
To Provide Notification of Deteriorating Performance

- Variation Over Time of Key Parameters.
- Output Signal Quality
- Power consumed
- Temperature Rise
- SNR/Eye Diagram

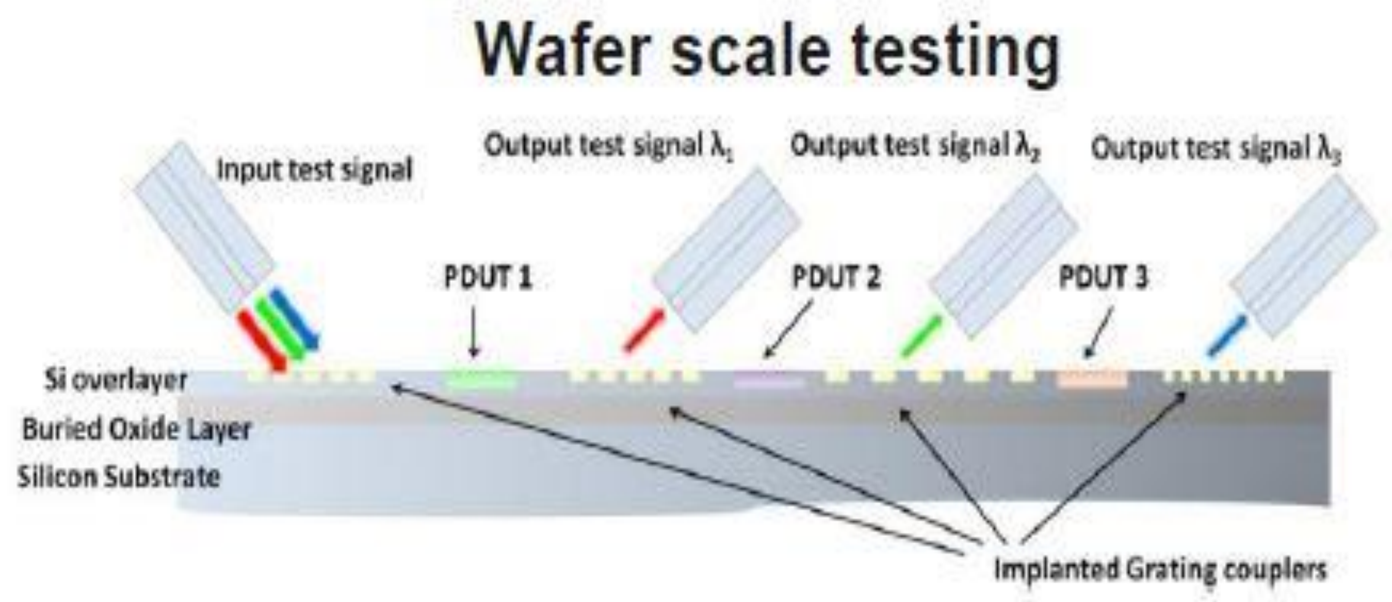
Optical Test vs Electrical Test

- Optical Signals have **more characteristics to measure** than Electrical Signals
  - Tends to take more time
  - More data to gather, record and analyze
- Optical Test Equipment is more Expensive
  - More parameters to measure
  - **Number of test sets bought is low**
- **Optical Test access is more difficult**
  - Beam Alignment (5 axis) vs contact (3 axis)
- Usually **no optical gain** in the PIC, so loopback, other electrical test “tricks” are more limited.

In summary, optical products are usually more complicated & costly to test than electronics.

- **Incoming Inspection (Difficult)**
  - Ensure parts and materials meet requirements
    - Dimensions, Surface finishes, Functional performance, etc.
    - **PIC die inspection is “hard”.**
  - Examples:
    - Fiber & trench inspection prior to assembly.
    - **Photonic Interposer metrology**
- **During Manufacturing (Often Not Done. Too expensive to Tool.)**
  - Ensure assembly processes are “robust” (i.e. Cpk >1.33)
  - Eliminate Defective in-process subassemblies when economically viable.
    - Does in process test save more than it costs ? Complex Question.
      - Is rework viable ?
- **Final Test (Necessary To ensure that only good devices are shipped.)**
  - Ensure final test yields are high, ideally 100%.

- Historic
  - Optical Connector, SM & MM
  - Temporary splice to a pigtail
  - Mode leakage
  - Focused Lens
- Emerging
  - Waveguide Edge/End
  - Grating on surface
  - Temporary grating
  - Evanescent coupling



Generic Optical Test Costs

- **One Time Expenses (Usually Big $!)**
  - **Developing tests**
  - **Buying test Equipment**
  - **Designing and/or buying test sockets & apparatus**
- Expense Per unit tested (Minimal, minimize)
  - Cost of DL Time to test each unit
- Maintaining Test Capability (Usually small)
  - Equipment Calibration & maintenance
  - Record Keeping
  - Data Analysis
- **Yield Loss (Continuous effort to minimize)**
  - **Cost of parts that fail**

Specific Optical Test Costs

- Testing Single Mode is More Expensive than Testing Multi Mode
  - **Tolerances force active alignment**
- Final Production of Modules, especially Telecom, DataCom
  - **BER, takes a long time**
  - **Cost of Equipment**
    - **Instruments**
    - **Fixtures for access**
- Work–In-Process In-Production, sub-assemblies
  - **Difficult to access optical ports & “fixture” for test**
- Chip level **(Widely needed so capability is developing)**
  - **When possible, Important to ensure die are good.**
  - **Wave guides are accessible at chip edges with effort**
  - **Gratings are being used**
- Wafer
  - Difficult to access optical ports

Optical Test Issues

- Choosing Production Test criteria that match the Need & Potential Faults
  - “Wisely” manage the Reach spec. to Reduce test cost.
    - BER Testing takes much Test Time.
    - Test time is increased by “stretching” the Require Reach, reducing SN and raising BER.
- Changing Optical Test Configurations is Difficult due to high mechanical tolerances.
- **Highly band-guard PIC die test criteria to minimize/eliminate later failure of high value products.**
- **Work-in-process testing is often not Cost Effective for Low Volume**
  - **expensive to implement.**

IPSR RoadMap Results

Test Challenges/Barriers, Unfilled Needs Potential Solutions, Test Gaps & Show Stoppers

Test Challenges/Barriers

- Designing the product for testing (end to end)
  - Self test
  - Self error correction
- **Providing optical test ports at the wafer and die level.**
- **Fiber alignment to sub micron tolerances is hard.**
- **Driving testing earlier into the process (wafer level)**
- Reducing test time (especially Bit Error rate)
- Utilization of loopback

Unfilled Optical Test Needs

- **Universal, Versatile Optical Test Port & Optical Probe Standards**
  - **Wafer and Die Level**
- Ability to test Photonic Properties of Wafers During Fab to Provide "Known Good Die".
- Flexible Test Platform, Compatible With the Needs of Multiple Applications.
- Processing Ever Faster (100Gbs+) Data Streams
  - limited by Memory IO Data Rates
- Optical Array Testing, especially as data rates increase
  - Accessing edge couplers
  - Measuring properties across the array
- Eventually, the Ability to Support 200 THz fiber date transfer Rates

Potential Solutions

- Build photonics test structures in/on wafer and test at the wafer level.
- Higher levels of integration
- Build fault tolerance/self-repair into the product during design
- **Develop high volume, versatile, single mode test access method for a manufacturing environment to provide optical ports.**

Test Gaps and Showstoppers

- Low speed of suitable assembly, test and other process equipment resulting in high costs. **"Time is money"**
- **Low Production Volume of Photonic Devices Makes recovery of investments, including test capability, hard; Result is high Amortized cost per device.**
- Designing for Manufacturing and test:
  - Maximizing output to reduce cost
  - Studying designs to trade off accuracy and speed

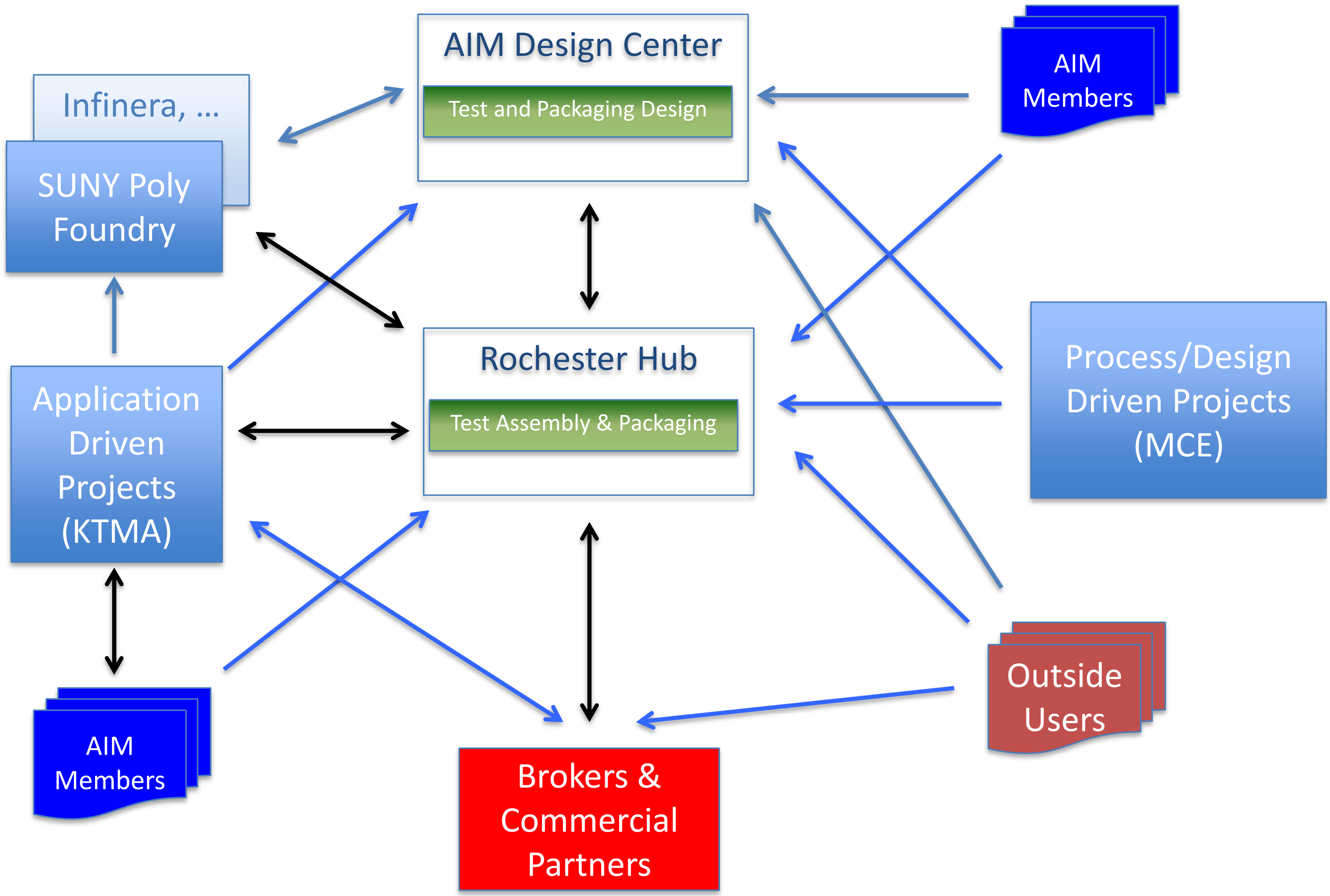
Limits resulting from adopting existing equipment, materials and methods to optical test. Specialized equipment is not available; demand is insufficient to incentivize equipment manufactures.

AIM-IP

Test Assembly Packaging (TAP) Capabilities

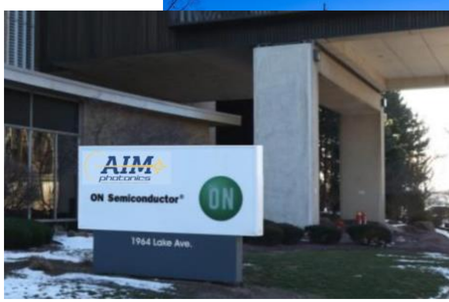
Rochester, NY

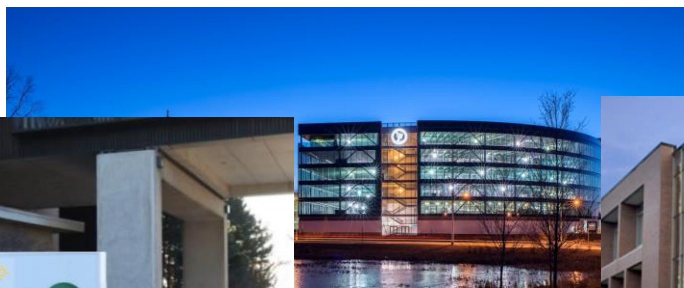
AIM Photonics information flow

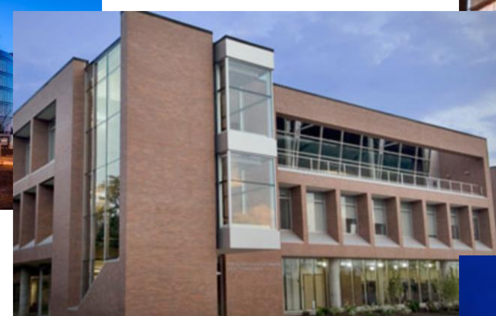


The Rochester Hub for Test, Assembly and Packaging

- Part of the AIM Photonics manufacturing consortium
- Emphasis on design for package, design for test
- Team: RIT, Univ. Rochester, SUNY Poly, Columbia







Combining wafer scale assembly with precision fiber attach using a holistic approach:

design for test;
design for package;
design for reliability

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- Emphasis on design for package, design for test
- Team: RIT, Univ. Rochester, SUNY Poly, Columbia





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The Test Assembly and Packaging Facility

Centrally accessible facility (mid 2018 move-in)

Complete tool set for
- SMT
- Metrology
- High speed/high throughput testing
- Photonic I/O
- Packaging Design

Space for R&D, Prototyping & Low Volume Production

Space for Workforce development

Space for (proprietary) company development projects

Metrology and testing in the packaging process

Wafers and Interposers arrive at TAP Facility Ready for processing

Wafer Solder Bumping
- Copper Sputtering
- Masking
- Plating
- Stripping
- Reflow to Balls
- Carrier attach
- Wafer Taping
- Wafer Debonding
- Wafer Dicing

Interposer Bumping
- Copper Sputtering
- Masking
- Plating
- Stripping
- Reflow to Balls

Bump Metrology
Wafer Thickness
Profilometry
Roughness

XRF

Die to Interposer
- Pick/Place good die onto interposer
- Thermal Bond die to interposer
- Tape
- Dice die/interposer structure
- Remove die/interposer from tape and place into trays

Interposer to Laminate
- Print solder on pads
- Pick and place interposer structure onto laminate
- Reflow to bond
- Underfill
- Cure
- Lead Frame
- Inspection
- Load into trays

CT X-Ray
Alignment
Acoustic Microscop

XRF
Acoustic Microscopy
CT X-ray

Solder Ball Laminate
- Print solder on pads
- Reflow to Balls
- Inspection
- Load into trays

Solder bumping

Fiber Attach
- Prep Fibers
- Attach Fibers
- Wire bond
- Inspection

Trench Inspection
Surface Inspection
Fiber Inspection

Encapsulate or Seal

Underfill/Overmold	Butterfly Pkg
Plasma Clean	Laser weld seal
Underfill/Overmold	Wire Bond
Cure	
Clean	
ID Mark	
Lead Frame	
Inspect for voids	

Coupling Loss
Backscatter
NIR Inspection
VIS Inspection
SEM Analysis
CT X-ray

Assemble to PWB
- Clean
- SMT
- Underfill
- Cure
- Inspection
- Load into Trays

Thermal Profiling
Differential Cal.
Optical inspection

Reliability
Shear/pull testing

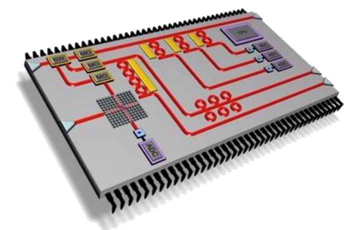
Envisioned Process Flow

Pre 2.5D | Post 2.5D | Pre Optical I/O | Post Optical I/O | Thermal Management | Standards & Reliability

Testing Capabilities of AIM Photonics

Baseline wafer and package level testing

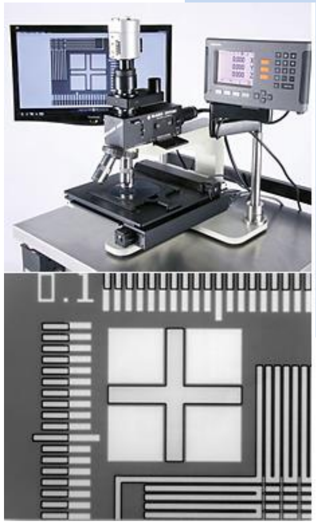
- Electrical Connectivity
- RF Bandwidth
- Photonic Connectivity
- System Functional Test

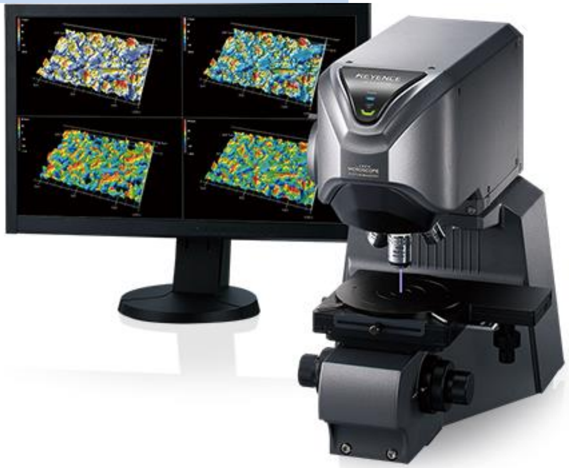


Chem/Bio sensing (at URMC Laboratories)

Packaging Metrology

- Multidimensional optical microscopy
- Scanning Electron Microscopy
- Acoustic Microscopy
- CT X-Ray Inspection

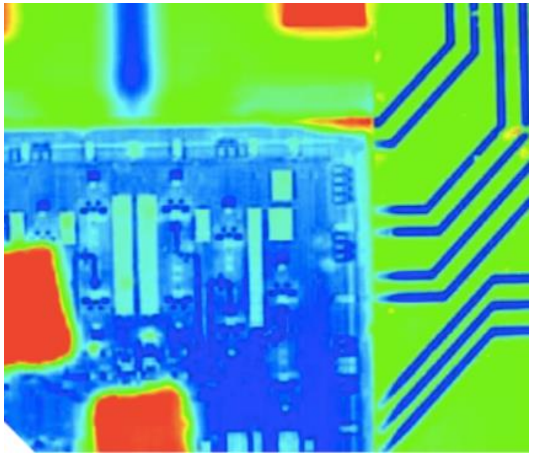




Testing Capabilities of AIM Photonics

Reliability Tests

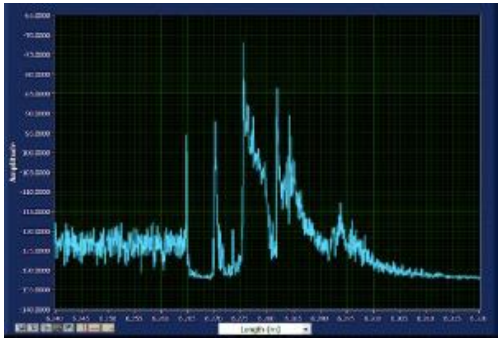
- Shear and Pull Testing
- Thermal Imaging



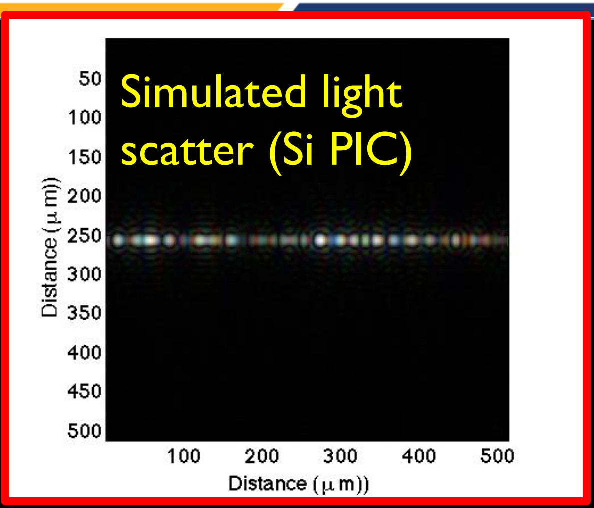
Connectivity Tests

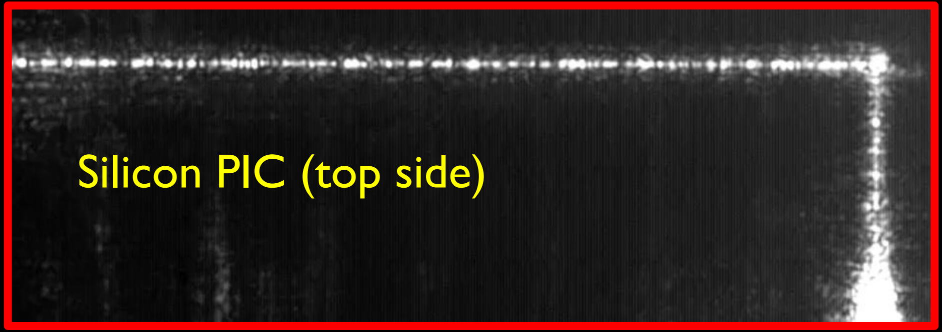
- Optical Backscatter
- SWIR Microscopy

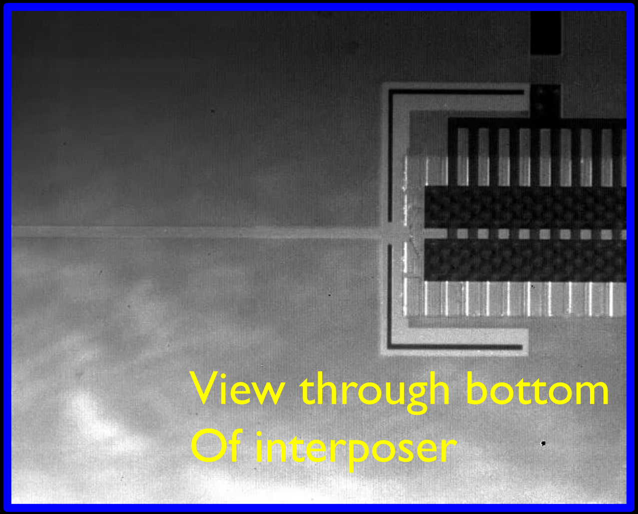
20 µm resolution in optical backscatter

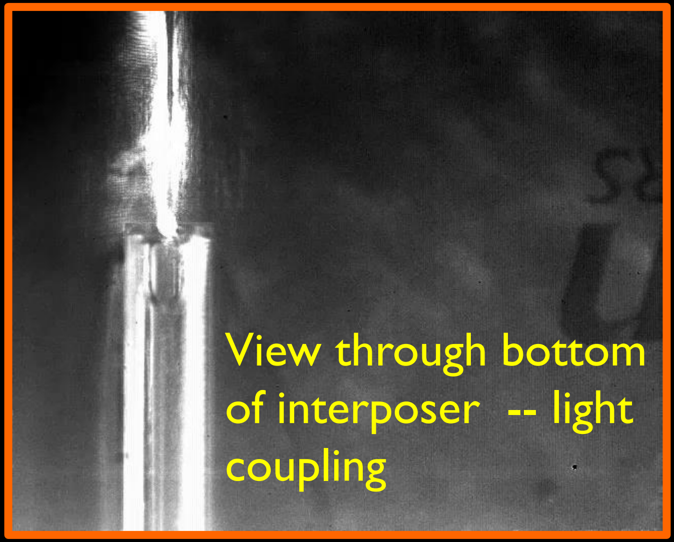


SWIR Microscopy & Light Scattering Spectroscopy









Baseline Testing – Connectivity, optical power, wavelength, detector quality (DC), baseline electrical performance, thermal management, etc.

Functional Test -- Application specific

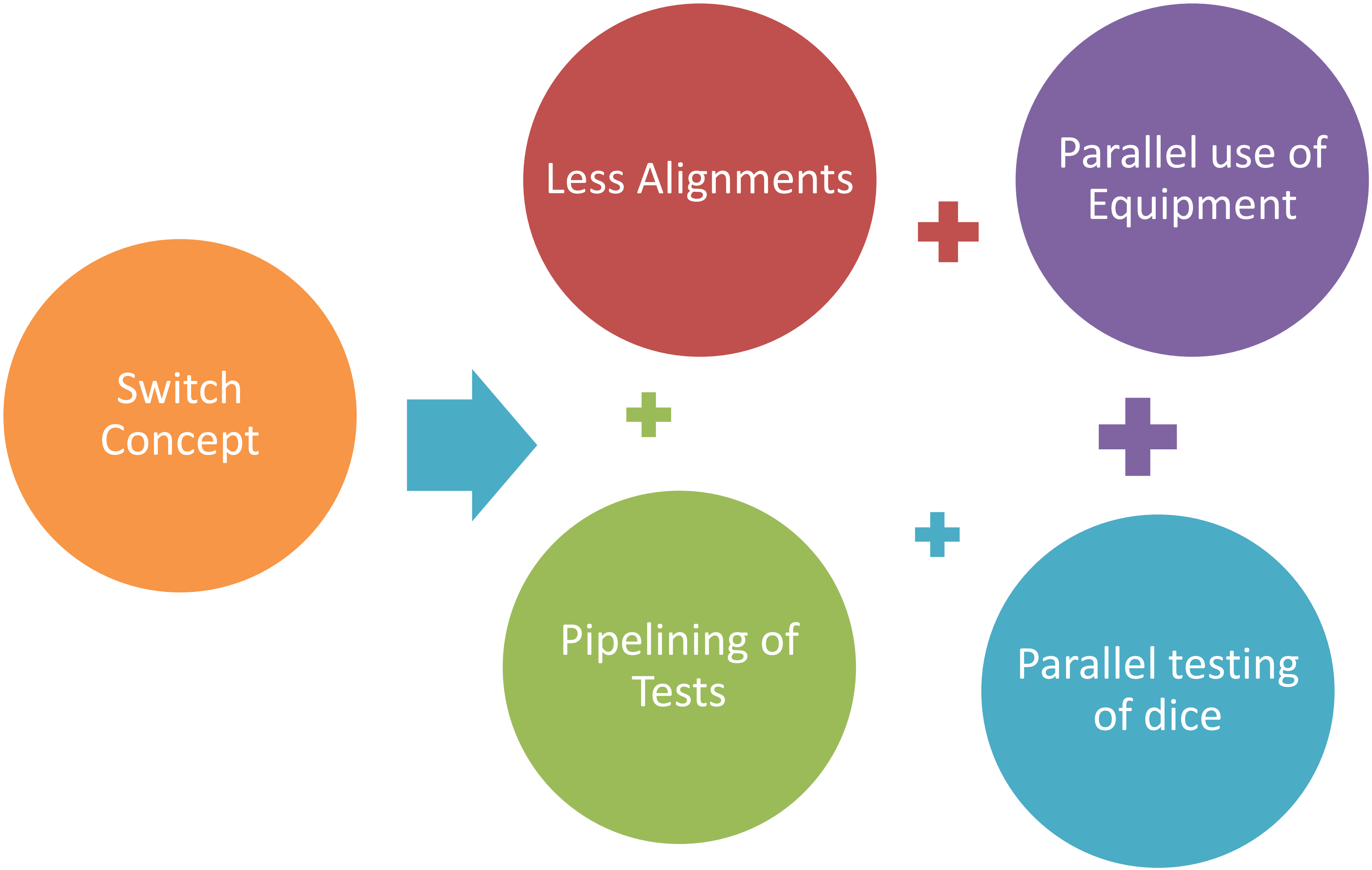
Datacom Example: Bandwidth, BERT, etc

Biosensor Example: Resonance wavelengths, pathogen sensing

Testing in AIM Photonics

Process Capabilities	**I/O Capabilities:** • Grating Coupler on wafer and chip scale • Edge Coupler on chip scale **Environmental Control:** • Temperature: Ambient to 80C **Parametric Optical Measurements**: • Injection Loss/Reflection Loss/Wavelength Dependence/Polarization Dependence/Cross Talk/Linewidth/Phase **Parametric Electrical Measurements:** • VI Curves **Hybrid Parametric Measurements:** • All correlation between upper measurements **RF Measurements:** • E/O and O/E device bandwidth / Eye Diagrams / Transition times / Constellation Measurements **Digital Communications Measurements:** • E/E, O/O, E/O, O/E Bit Error Rate Measurements

Incorporating a Measurement Switch



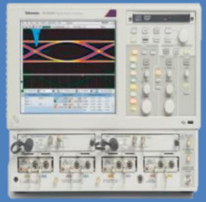
Top of Measurement Switch (Concept)

Equipment Rack:

(c) Keysight

(c) Anritsu

(c)OptoTest

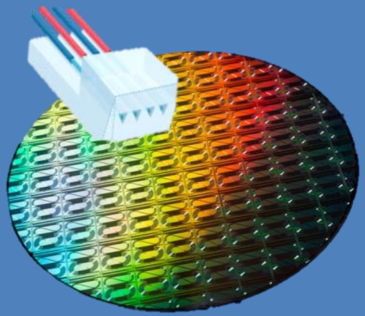


(c) Tektronix

Optical Switching Unit

INPUT: / OUTPUT:	Laser	PPG	Power Meter	Oscilloscope	Splitter In	Splitter Out 1	...	Splitter Out N	Fiber Array 1	Fiber Array 2	...	Fiber Array N
Laser												
PPG												
Power Meter											X	
Oscilloscope												X
Splitter In												
Splitter Out 1												
...												
Splitter Out 2												
Fiber Array 1	X											
Fiber Array 2		X										
...												
Fiber Array N												

Wafer Prober:



(c) TDK
(c) MIT - Bryce Vickmark

ProberControl - Framework

Orchestrate Tools for complex Measurements

Interact with Wafer Tester

Schedule Measurements

Direct Command Execution on Tools

Visualize Results

Classify Chips based on Results

Get it from www.github.com/ProberControl/ProberControl

Design for Test

Obey the I/O standards

Reduction of Complexity, Integration of Processes

Cost reduction (minimizes retooling)

Understand Parameterization Sets

DC Tests of devices and subcircuits

Ex: 20 grating couplers at 127 μm pitch

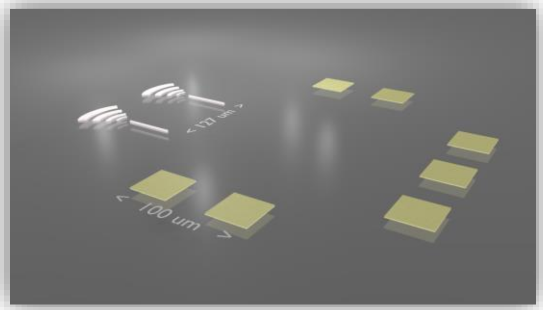
25 pads at 100 μm pitch

Distance between lines > 300 μm

Design for Test

Functional Sets

- Used for high speed tests
  - Ex: 2 Optical I/O + 2 x 2 DC + GSG RF
    - 4 Optical I/O + 2 x 5 DC + GSGSG RF
    - 20 Optical I/O + 2 x 25 DC + GSGSGSGSG RF
- Minimum and Maximum distances apply
  - (but positions can be varied)



- Optical I/O for testing can be either grating or edge couplers

Testing ports can (sometimes) be used for optical I/O in packaging

Test Assembly and Packaging in AIM Photonics includes

- Facility planning and management (Ed White)
- Tool purchase and qualification (Team)
- Design for package, design for test (Team)
- Architectures (Hardware, Software, Data Management)
  For programmed (automated) testing & assembly
- Metrology tooling for package analysis
- Process development for Optical I/O, Metrology, Test.

Team: Keren Bergman, Robert Polster, Columbia Univ.
Stefan Preble, Donald Figer, RIT
Ed White, Tom Miller, Anthony Lisi, SUNY Poly
Thomas Brown, Ben Miller, Jaime Cardenas, University of Rochester
Alan Evans, Corning
Justin Bickford, DoD (ARL)

Questions ??

thomas.brown@rochester.edu
Otte@promex-ind.com

https://aimphotonics.academy/roadmap/ipsr-roadmap

http://www.aimphotonics.com/tap-facility/

http://www.aimphotonics.com/