Integrated Photonics
Grand Challenges and Key Needs for 2018

Lionel C. Kimerling
MIT
AIM Photonics Institute

IPSR-International Webinar: December 21, 2017

Data Centers – 3D/Augmented Reality/Automotive – 5G/IoT

integration – standardization – cross-market platforms
- Integrated Photonics Technology supply chain

Link to webinar recording (good for six months after event): http://bit.ly/2lWqt3t

Challenges and Needs for 2018

- **Critical Themes (3-10)**
  - *Functional Blocks* - Platforms – System Level Design
- **Economics (10-16)**
  - *Demand* – Component-to-System Cost - Reliability
- **Technology (17-30)**
  - TxRx (DC) - RF Signal Processing (5G) - *e-p Synergy*
  - *Sense: sampling and signal interpretation*
- **Manufacturing (31-34)**
  - *Standardization* – Consolidation - **Coordination**
- **Success in 2018 (35-36)**
  - *Continuity*: electronics-photonics-integration

Outline: Economics, Technology, Manufacturing

Supply Chain Coordination: Mobile 3D

Infrared laser projector components: i) a vertical-cavity surface-emitting laser or edge-emitting laser, ii) wafer-level optics, and iii) diffractive optical elements.

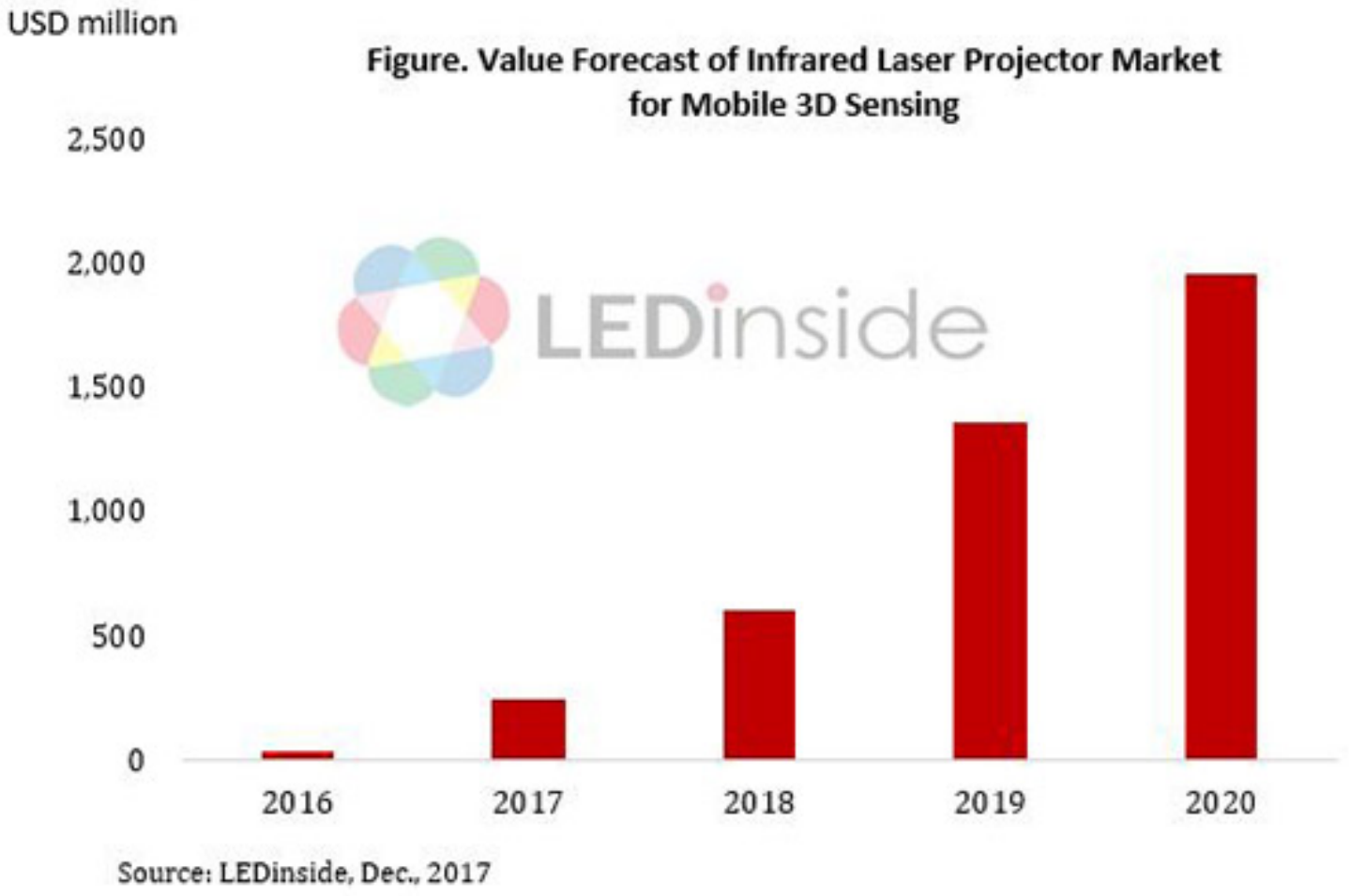


Figure. Value Forecast of Infrared Laser Projector Market for Mobile 3D Sensing

Source: LEDinside, Dec., 2017

Technologies: multipoint CMOS imaging; ToF mapping; structured light; phased arrays.

Outline: Economics, Technology, Manufacturing

Silicon Photonics Datacom Vision

Cable – Board – Package - Chip

2015-16	2017-20	2020-25	Beyond
Discrete Devices	Interposers	EO CPU/ASIC	Logic-Memory-IO Integrated SiPh SoC Photonic Systems
EO Transceivers	InP VCSEL	Si Lasers	
Interconnect Modules	EO SiP/PoP	Multi-Die SiP	
MM Connectors	Fly-Over Cables	EO/Waveguide PCB	Wafer-Panel Substrates
MM Cables	MM-SM Connectors	SM Connectors	IO Connectors
AOCs	MM-SM AOC	SM Cables	Future WG

Interconnects Packaging SiPh Integration

Silicon Photonics is the "future proof", modular solution for SM-WDM bandwidth density scaling.

- increases: yield, reliability, density
- reduces: cost, *time to market*, power, latency

Integrated Photonic Systems Roadmap 2016

Integrated Photonics: 2018 Priorities

- **Automated Design**
  - validated PDK models: e-p circuits and systems
  - foundry infrastructure: IP licensing/indemnification
- **Monolithic Integration**
  - heterogeneous SM functional blocks
- **Optical Packaging**
  - on-chip/off-chip; interposer; on-board parallelism
  - parts supply chain; known failure modes
- **Test**
  - Design-for-Test; BIST; high throughput

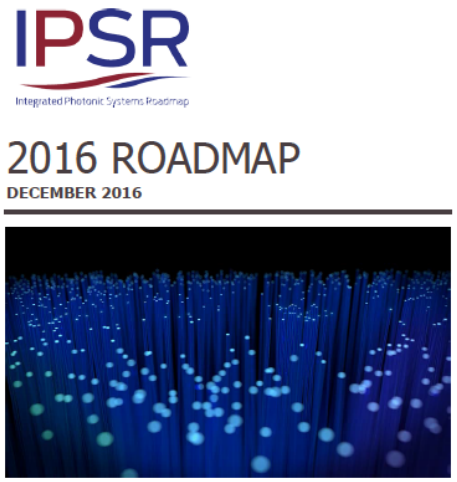
The Road to Silicon e-p Synergy

Technology	Status
2015-16	
GaAs Lasers	VCSEL arrays commercially deployed in datacom
InP Lasers	Edge emitter arrays commercially deployed in telecom
Ge-on-Si Lasers	Research demonstration by several labs
Ge-on-Si Detectors	Fully waveguide integrated, commercially deployed
Waveguides	Si, SiON, SiN commercially deployed
SiP/SoC Assembly Technology	Electronics, but not photonics
Si Photonic Integration	Commercially deployed in cable and board assemblies
2017-20 Projected	
Ge-on-Si Lasers	Early market entry
Ge-on-Si Detectors	Pervasive commercial deployment
Waveguides	Pervasive commercial deployment; single channel
SiP/SoC Assembly Technology	Early 2.5 D deployment
Si Photonic Integration	Pervasive commercial deployment: cables and boards
2020-25	
Waveguides	Pervasive commercial deployment: WDM
SiP/SoC Assembly Technology	Pervasive commercial deployment: cables and boards
Si Photonic Integration	Emerging chip-to-chip intra-package
Beyond	
SoC Assembly Technology	Embedded in distributed circuit/system architectures
Si Photonic Integration	Transceiver-less: embedded electronic-photonic synergy

700 contributors

254 organizations

16 countries



10/17 TWG updates

InP, SiN (GaN) are important to an emerging heterogeneous e-p platform.

Outline: Economics, Technology, Manufacturing

Supply Chain Coordination

Table 3. Integrated Waveguide Roadmap

Key Attribute	Parameter	Description	2016	2018	2020	2025	2035
Transparency	dB/cm	attenuation/distance	0.35	0.1	0.05	0.001	0.001
Material	n	effective index	1.8-4	1.8-4	1.8-4	1.8-4.	1.8-4.
Index Contrast	Δn	n(core) - n(clad)	10^{-3}-3	10^{-3}-3	10^{-3}-3	10^{-3}-3	10^{-3}-3
Stability	pm/°K	spectral shift of resonator	*25*	*1*	*1*	*0.5*	*0.01*
Power	mW	optical power capacity	30mW	30mW	50mW	100mW	500mW
Wafer Uniformity	nm	layer thickness variation	10nm	1nm	1nm	0.5nm	0.5nm
Material System	Core /Clad	waveguide and clad materials	Si,SiN /SiO_2	Si,SiN, Ge,ChG /polymer, SiO_2,ChG	multilayer	multilayer	multilayer

- Extend this table to ***3D waveguide (industry expects this to happen by 2020)***
- Extend this table to independently ***routable optical layers*** (vertically integrated WG)
- ***Integration level complexity*** to be added
- Study ***cost scaling at system level***

Ajey Jacob, Global Foundries
co-chair, Monolithic Integration TWG

Outline: Economics, Technology, Manufacturing

Supply Chain Coordination

Table 5. Photodetector integration roadmap

Key Attribute	Parameter	Description	2016	2018	2020	2025	2035
Absorption	α (cm^{-1})	loss @ 1550nm	10^3	10^4	10^4	10^4	10^4
Dark Current	I (nA)	interface + bulk	0.2	0.1	0.1	0.1	0.1
Process Integration	cm^{-2}	dislocation density	10^7	10^7	10^6	$<10^5$	0
Efficiency (p-i-n)	R (A/W)	responsivity	1	1.1	1.1	1.1	1.1
Bandwidth (p-i-n)	B (GHz)	B @ 1550nm	40	67	100	100	100
Gain x Bandwidth (APD)	GB (GHz)	GB @ 1550nm	300	400	--	--	--
Guided Power	mW	~linear response	30mW	100mW	100mW	100mW	100mW

Table 6. Modulator integration roadmap

Key Attribute	Parameter	Description	2016	2018	2020	2025	2035
Baud Rate	Gb/s	OOK rate	25	50	50	100	100
ExtinctionRatio/InsertionLoss	dB/dB	Δα/α	2	2.5	3	--	--
Spectral Range	nm	@ Δα/α spec	25	25	25	25	25
Spectral Efficiency	b/Hz	DP-QAM	2	2	4	8	8

To be added in 2018:

specification of Materials and Tool performance

Ajey Jacob, Global Foundries
co-chair, Monolithic Integration TWG

Outline: Economics, Technology, Manufacturing

Supply Chain Coordination

Table 7. Laser, Gain Block, Optical Switch integration roadmap

Key Attribute	Parameter	Description	*2016*	*2018*	*2020*	*2025*	*2035*
Coupled Power	mW	waveguide coupled	1	5	20	30	30
Spectral Range	nm	1200, 1310, 1550	+/-10	+/-10	+/-10	+/-10	+/-10
Temperature Stability	pm/K, mW/K	wavelength, power	*5*	*1*	*1*	*0.5*	*0.01*
Package Integration	optical power supply	wall plug, package or waveguide integration	*2D ext*	*2D ext*	*2D hybrid*	*regulated wall plug*	e-p monolithic
Reliability	MTTF (hrs)	component life	10^4	10^4	$3x10^4$	$3x10^4$	10^5

Long discussion on reliability.
Agreed to keep the current numbers.

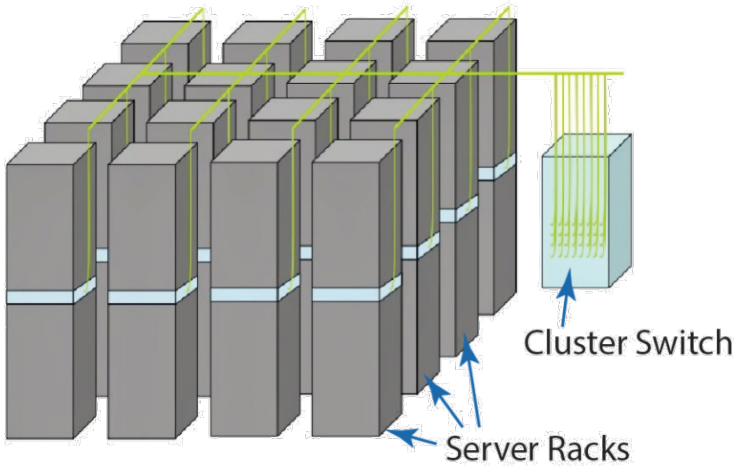
Ajey Jacob, Global Foundries
co-chair, Monolithic Integration TWG

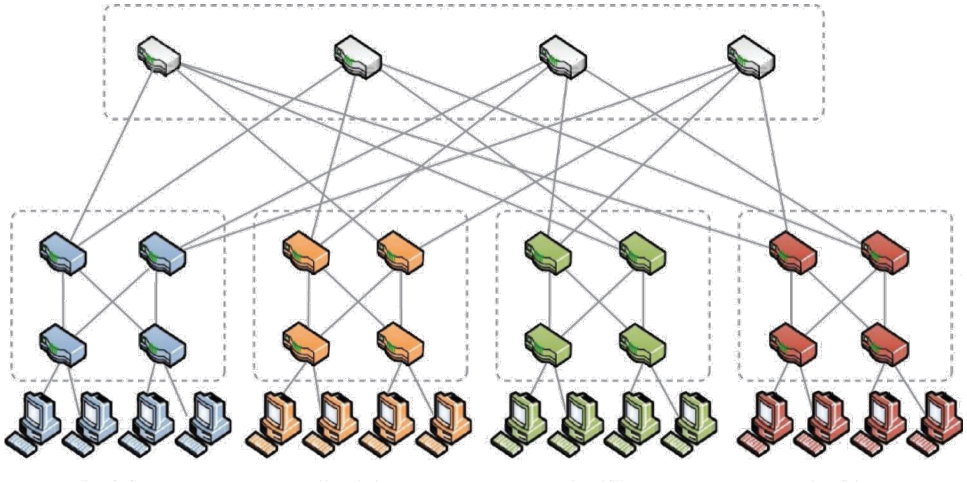
Outline: Economics, Technology, Manufacturing ***... Questions?***

Datacom Economics

- Will the **Data Center market** support the required R&D and drive adoption of integrated photonic technology?
- Key needs
  - platforms that leverage R&D investments
  - standards that limit R&D risk
  - manufacturing infrastructure for high volume ramp

Case Study: Transceiver





Hardware

Server Racks, Switches, Optical Transceivers, Fibers, Building Facilities (Shell, Power Supply, Cooling)

Software

Platform-level Software, Cluster-level Software, Application-level Software

+

Set-up and Operation

Development, Purchase, Installation, Electricity, Maintenance

Barroso, Luis Andre, Jimmy Clidaras, and Urs Hoelzle. The Datacen`ter as a Computer: A`n Introduction to the Design of Warehouse-Scale Machines. Morgan & Claypool, 2013.

The transceiver is part of the Data Center system.

W. Yu and R. Kirchain, MIT

Standardization Scenario

$ sales to support R&D cost of *one new product*

For an estimated Silicon Photonics TAM of $200M, the industry product cycle is 1yr for one product!

For estimated Silicon Photonics revenues of $30M for one company, the product cycle is 3.3yrs!

W. Yu and R. Kirchain, MIT

Cross-Market Platform Scenario

Can sales from the Data Center sector support *all new industry TxRx products*?

	# of Datacenters	Bisection Bandwidth Pb/s	# of layers of transceivers	$/Gbps per transceiver	$M transceiver sales	# of Products such sales can support
Google	15	5.2	4	1	312	1.5
Amazon	44	5.2	4	1	915.2	4.5
Microsoft	36	5.2	4	1	748.8	2.8
Facebook	~10	5.2	4	1	208	1.0

200G
400G
x
2 channels
4 channels
8 channels
x
OSFP
QSFP-DD
COBO
x
Si
InP
= 36 products >>

Mega-DCs can support 10 products each year.

1. High R&D cost + Market Fragmentation will support 36 product cycles of 3.6 yrs.

W. Yu and R. Kirchain, MIT

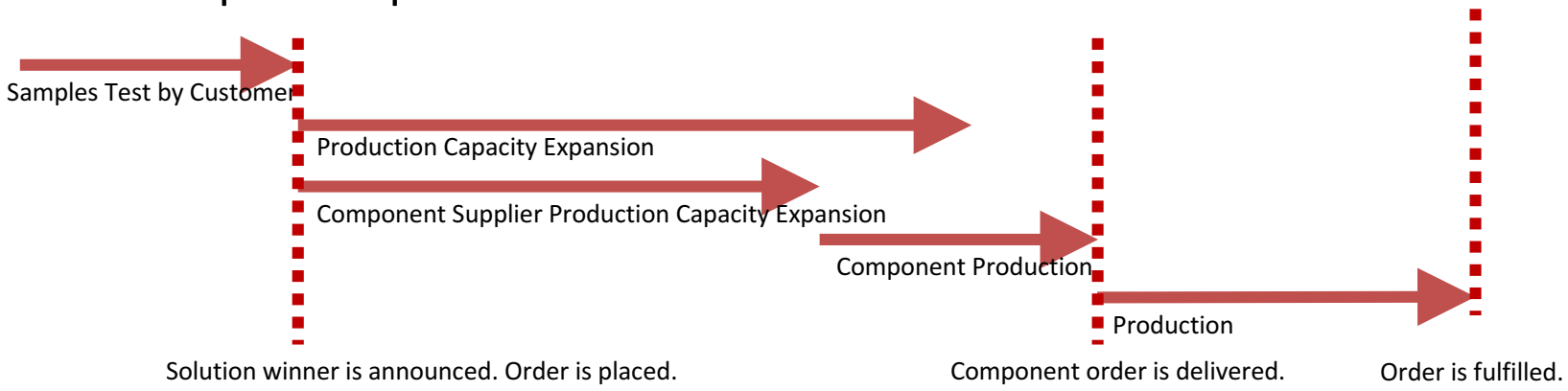
Manufacturing Capacity Ramp

- **Shortage of components**

  "Shortages of high-end optics, such as EML and DFB laser chips, is the main limiting factor for 100GbE market growth in 2016." – *LightCounting.com*

- **Limited production capacity**
  - High risk to make a multi-million investment before the accepted solution is announced.
  - It takes time to add equipment and people into production line.

"People assumed they had time to ramp…[but] the industry has never seen such a ramp with optics ." – *Andreas Bechtolsheim*

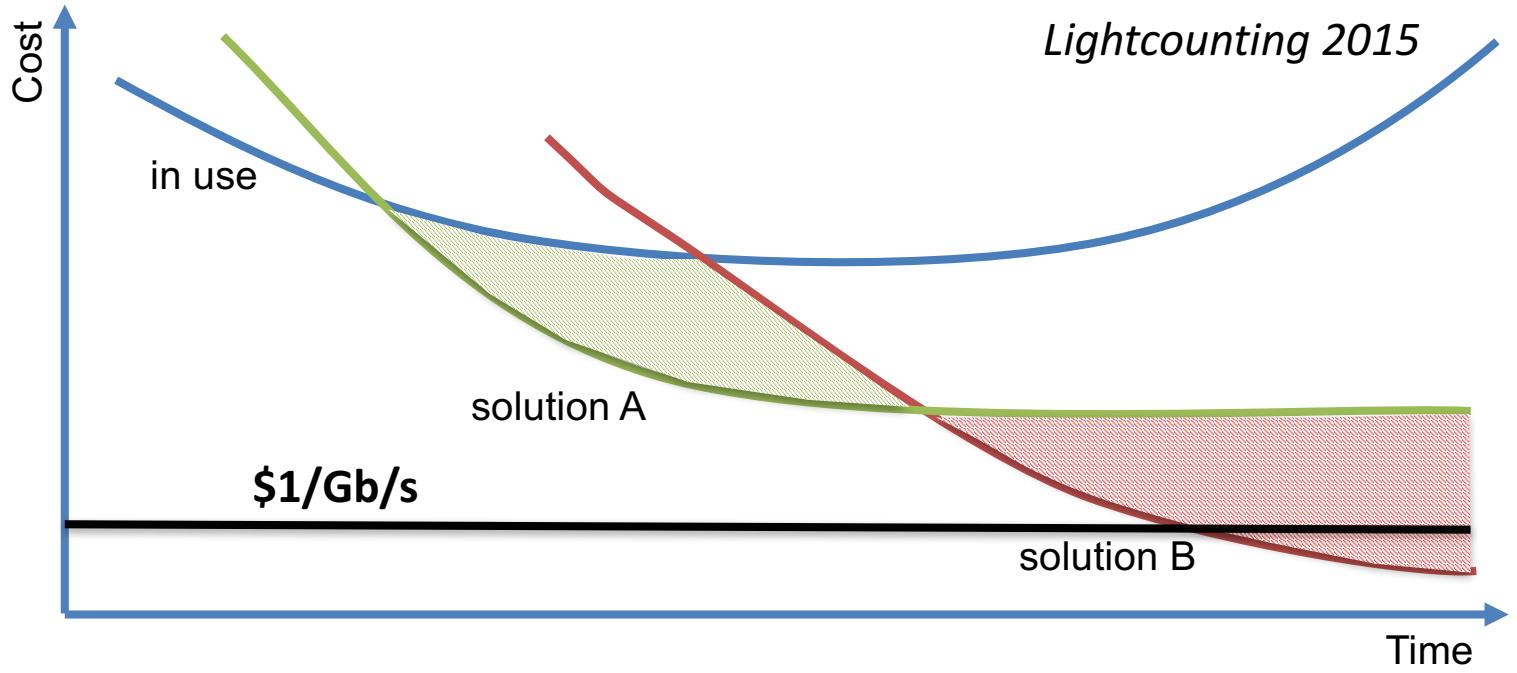


2. Production ramp time to high volume production limits revenue.

W. Yu and R. Kirchain, MIT

DC Scaling: Cost and Time

Data Center Connectivity TAM			
Year	**2016**	**2018**	**2020**
Revenues	$1.2B	$2.1B	$5.1B



R&D costs and production ramp rate determine Data Center revenue portion for integrated photonics.

- ***Cost and $/Gb/s will decrease with each new product technology.***
- ***Ramp time to high volume production limits revenue.***

W. Yu and R. Kirchain, MIT

TxRx Economics Summary

- **The optical transceiver is a bottleneck due to cost and time.**
  - *Cost* is i) device cost with ii) full implementation cost of that technology solution.
  - *Time* is i) time to sample plus ii) ramp time to high volume implementation.

- **Supply Chain coordination is critical to high volume production.**
  - Vendor and upstream supplier coordination
    - solution winner, *time scales* and volume.

- **The winning product should have an optimal combination of:**
  - performance, cost and *manufacturing scalability*.

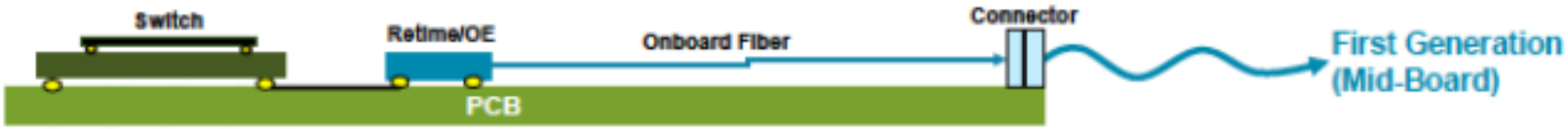
Building cross-market platforms

- **Transceivers**
  - *the transition to on-board optical interconnection*
  - MT connectors
  - optical interposers technology and cost
- **Analog RF optical signal processing**
  - transceivers: phase modulation
  - special purpose FFT processor: frequency channelization
- **Drivers for high level photonic integration**
  - coherent optical circuits
  - on-chip optical networks
- **Sensing and Optical Phased Arrays (>2018 AIM targets)**

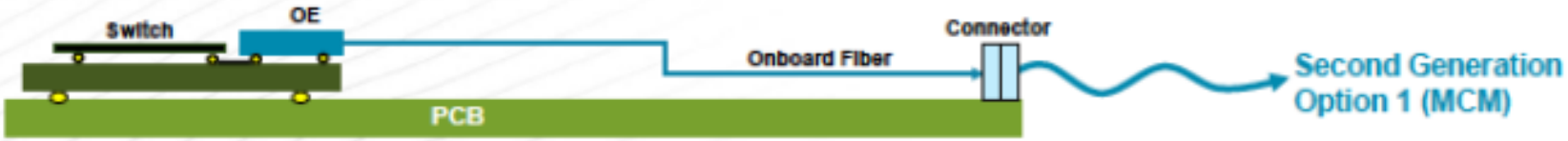
Frontier: Board Level Photonics

- Pluggable module with VSR/CAUI-4 interface may require two retimers

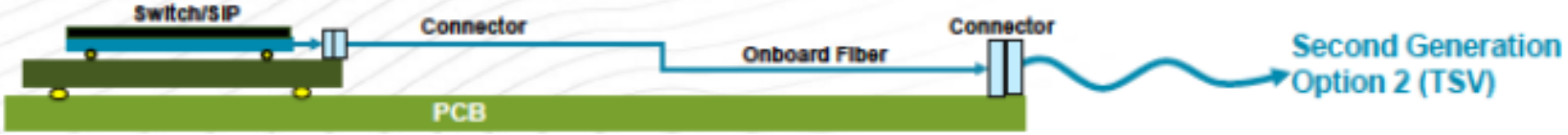
- SiP/optical engine connected to switch though PCB may require retiming



- SiP/optical engine mounted on the package does not require retiming



- SiP connected to switch though TSV does not require retiming



Sequence of line card implementations for increased bandwidth

Nicholas Ilyadis, Broadcom

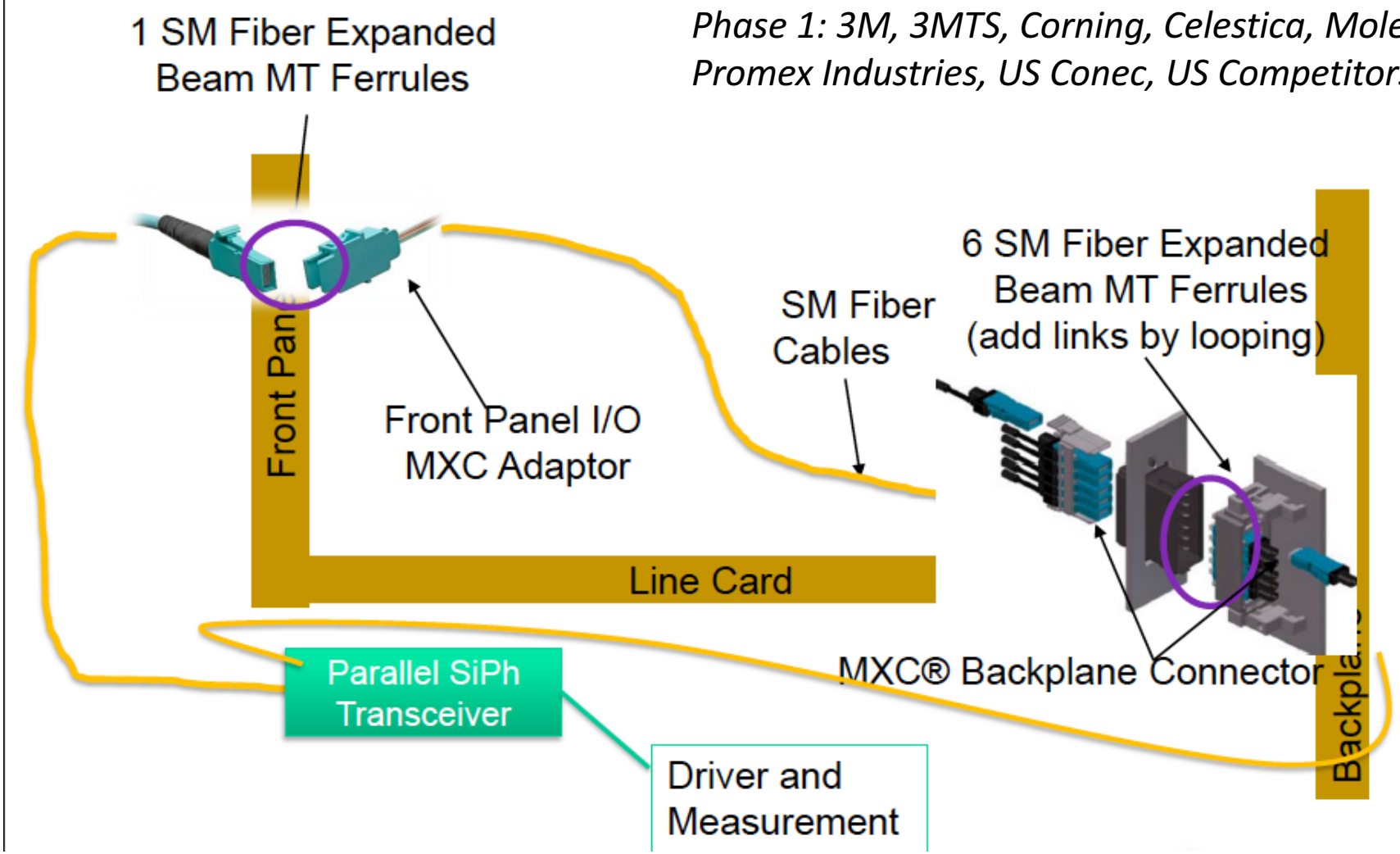
On-Board Optical Interconnection

- **Before the benefits of silicon photonics can be realized, new high performance and cost effective solutions to optical packaging and connectorization must be developed.**
- Optimum performance and functionality from silicon photonic devices and circuits require single mode (SM).
- SM requires precision alignment inside the package and in optical connectors.
  - expanded-beam (10um expanded to 80um) optical connectors relieve alignment and dust limitations
  - early entry for MM at short reach?

Optical interfaces degrade performance and increase cost.

Tom Marrapode, Molex

On-Board Optical Interconnection AIG



OBO AIG (Application Interest Group): 12 companies, international

Phase 1 complete in 2017; Phase 2 in 2018

On-Board Optical Interconnection

System Requirements

- Single-mode operation at SiPh operating wavelengths [1300, 1550 nm]
- Low propagation loss at SiPh operating wavelengths [<~ 0.01 dB/cm]
- Low polarization dependent loss (PDL) [< 0.1 dB]
- Low-loss coupling to standard SM fibers
- Transceiver-to-transceiver loss small [<~ 3 dB]
- Ease of termination (low cost) in connectors and sockets
- Ease of routing from mid-board modules to board-edge connectors.
- Low sensitivity of optical properties to temperature & humidity
- Reflow compatibility (if embedded in PCB) [260 C]

On-Board optical interconnection is an unsolved system problem.

Terry Smith, 3M

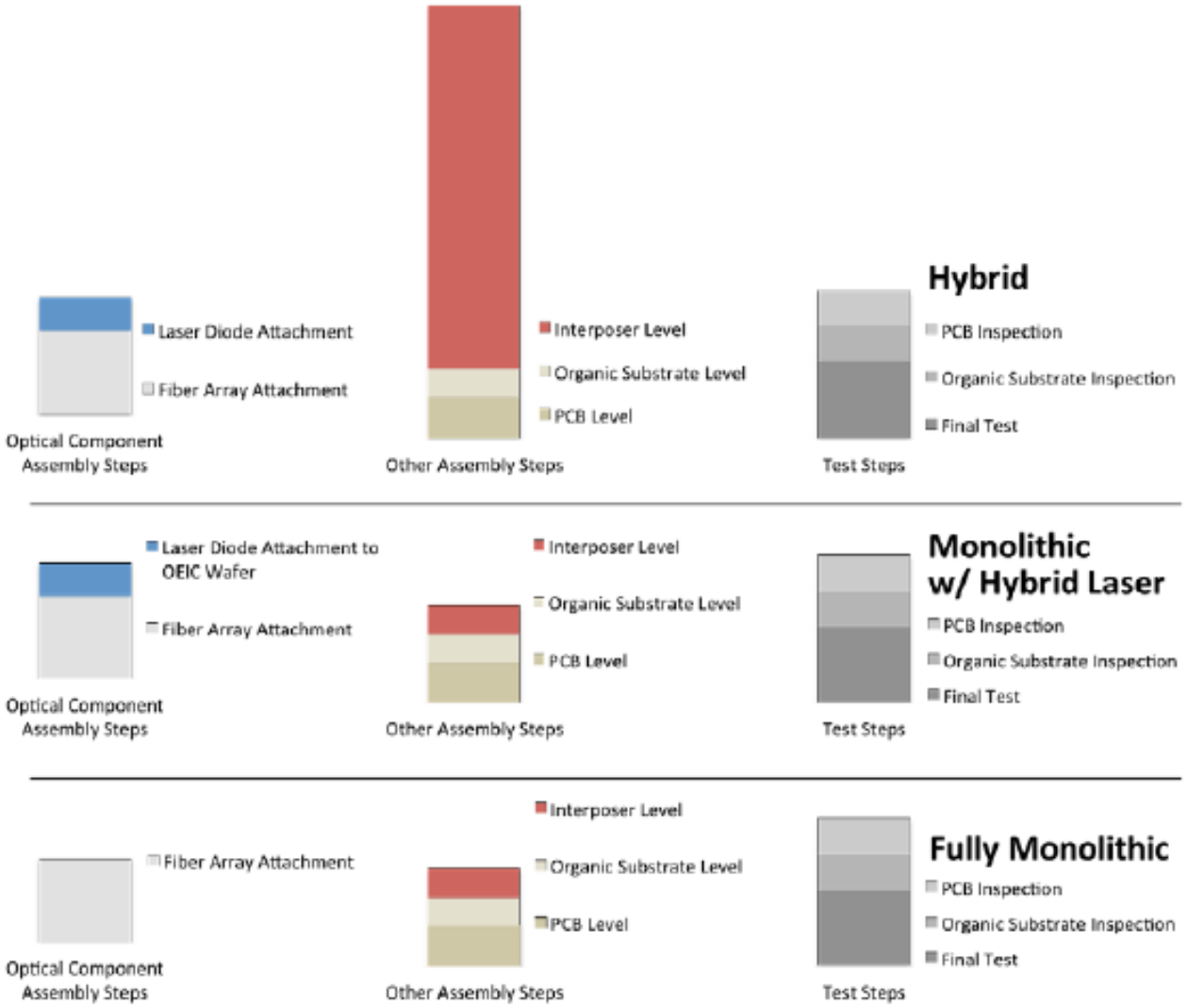
Challenge: Optical Interposer

The purpose of an interposer is i) to spread a connection to a wider pitch, ii) to reroute a connection to a different connection, iii) to enhanced reliability and assure successful assembly.

- Needs low-loss waveguides (but easier than PCB)
- Needs new, cost-effective low-loss optical-coupling bond between photonic components and interposer waveguides.
- Increases system parts count.
- Increases system process steps.
- May require special handling (due to fragility, temperature sensitivity, etc.)
- May require manual attachment to PCB.

Terry Smith, 3M

Assembly and Test Costs



Interposer Assembly Dominates Package Cost.

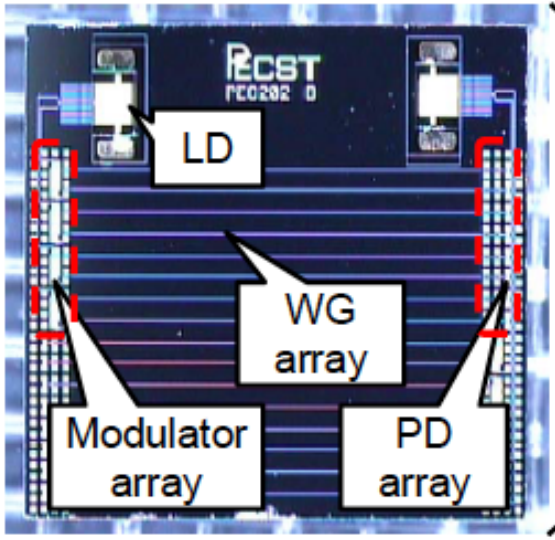
W. Yu and R. Kirchain, MIT

Technology: TxRx

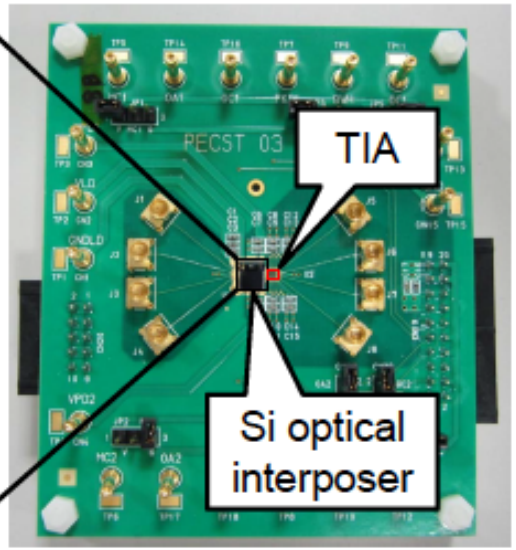
Functional Blocks

- **Transceiver**
  - power, bandwidth density
  - modulation format, polarization, spectral efficiency
- **RF Optical Signal Processor**
  - power, bandwidth density
  - notch filter, FFT
- **WDM Front End**
  - power, bandwidth density
  - temperature stabilization, e-p lambda lock

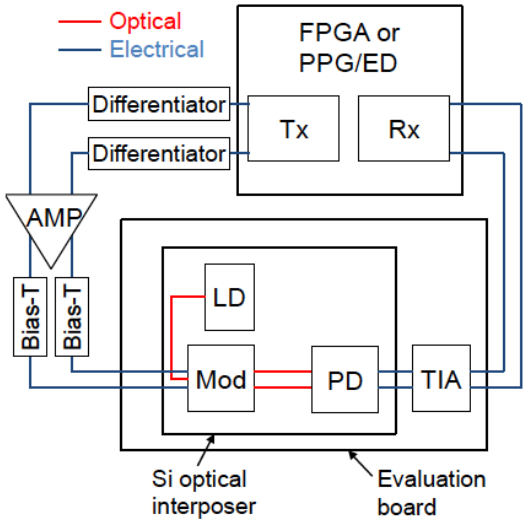
Interposer for FPGA Transceiver



Silicon Optical Interposer



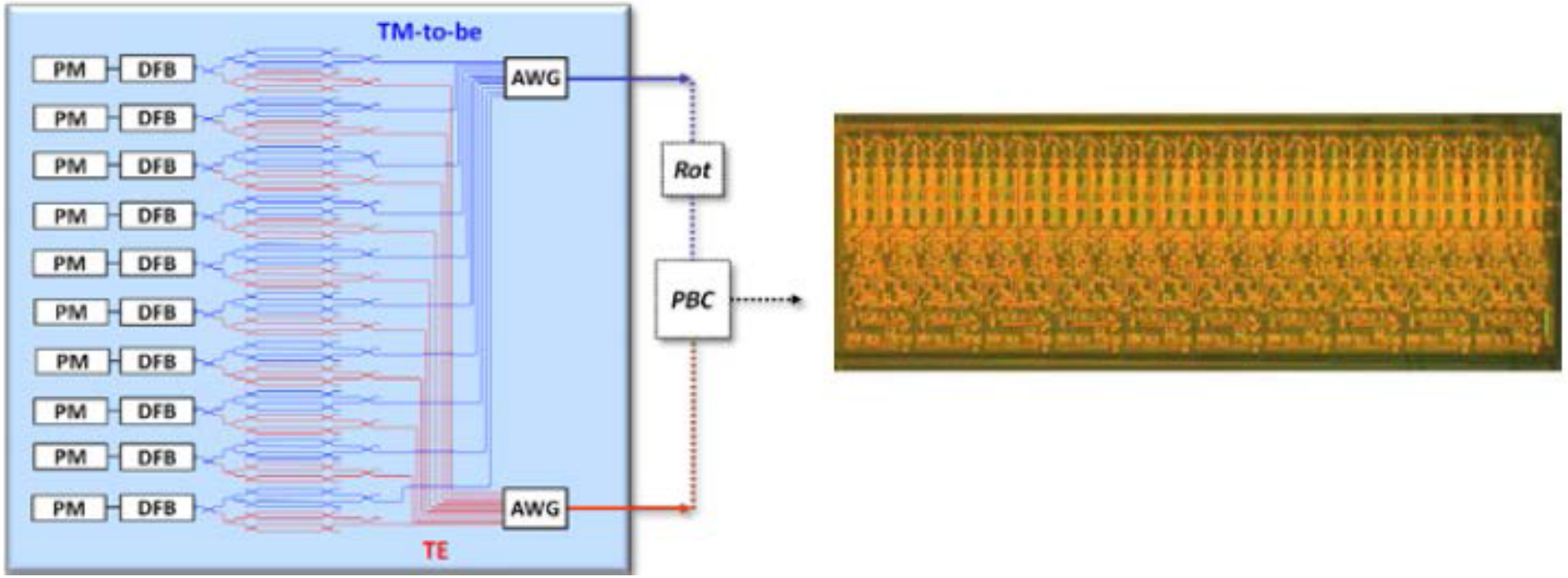
Link Evaluation Board



Test Schematic

- 25-Gbps error-free data link on a silicon optical interposer with an FPGA
- Transmitter pre-emphasis and receiver equalization
- Compatible with optical interconnect standards: OIF CEI-25G, 100GbE, 400GbE
- *Optical-pin/MM near term implementation*

D. Okamoto, et. al., "Demonstration of 25-Gbps Optical Data Links on Silicon Optical Interposer Using FPGA Transceiver", ECOC 2014. (PETRA, Japan)



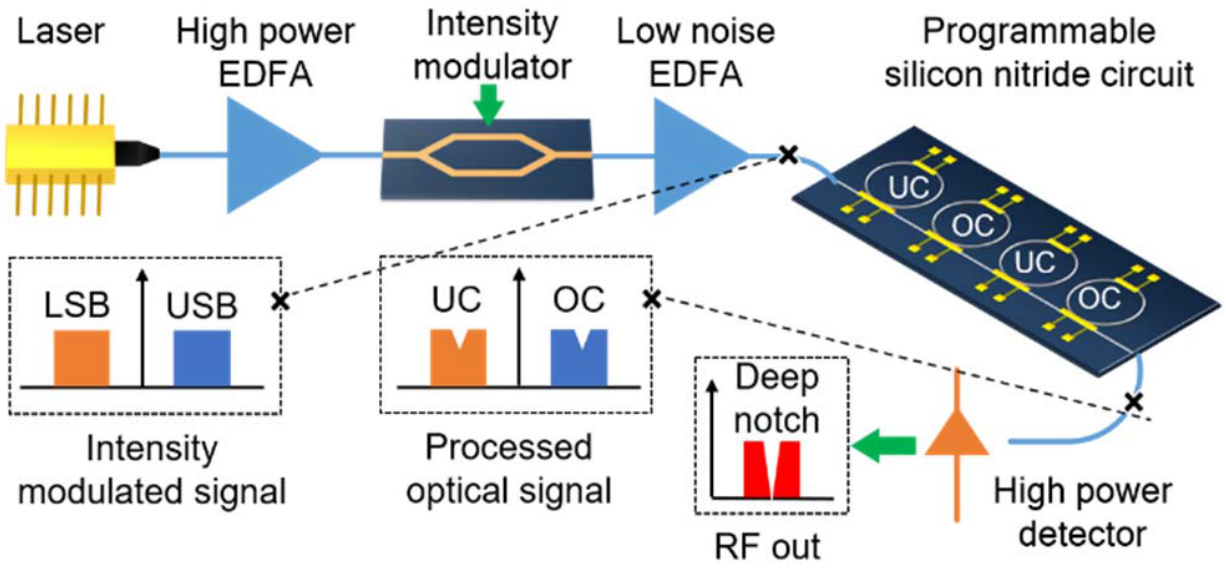
Schematic diagram of an InP-based 500Gb/s PM-QPSK transmitter PIC and the active block PIC on the right.

- ***10 tunable distributed feedback lasers***
- ***40 Mach-Zehnder modulators***
- ***all required sense and control electronics.***

Fred Kish, Infinera)

Integrated RF photonic filter

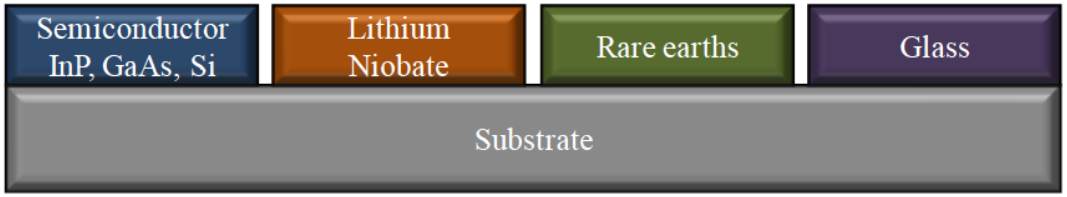
- low-loss silicon nitride circuit: ring resonators for pre-processing and optical filtering units
- low biasing of Mach-Zehnder modulator for link optimization to achieve low NF

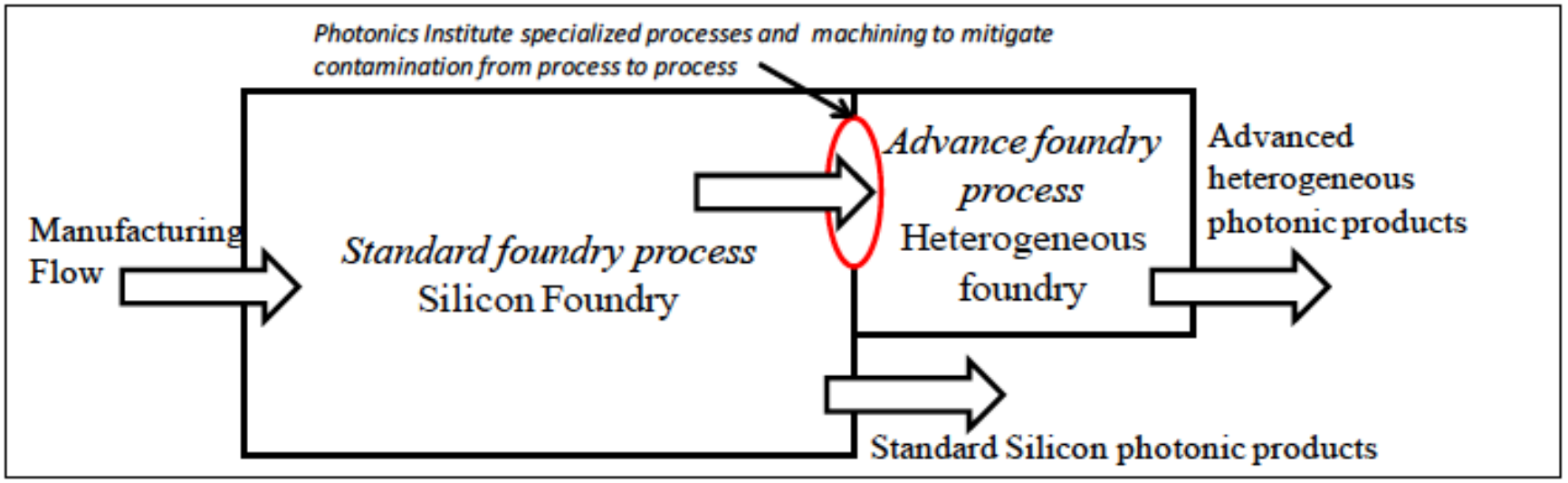


- **8 dB RF gain**
- **noise figure: 15.6 dB**
- **spurious-free dynamic range: 116 dB**
- **rejection >50 dB in the stopbands**

"Lossless integrated RF photonic filter with record-low noise figure and 116 dB of dynamic range", Liu, et.al., CLEO Pacific Rim 2017 and Opt. Lett. 42, 4631-4634 (2017)

Heterogeneous RF Photonics Platform



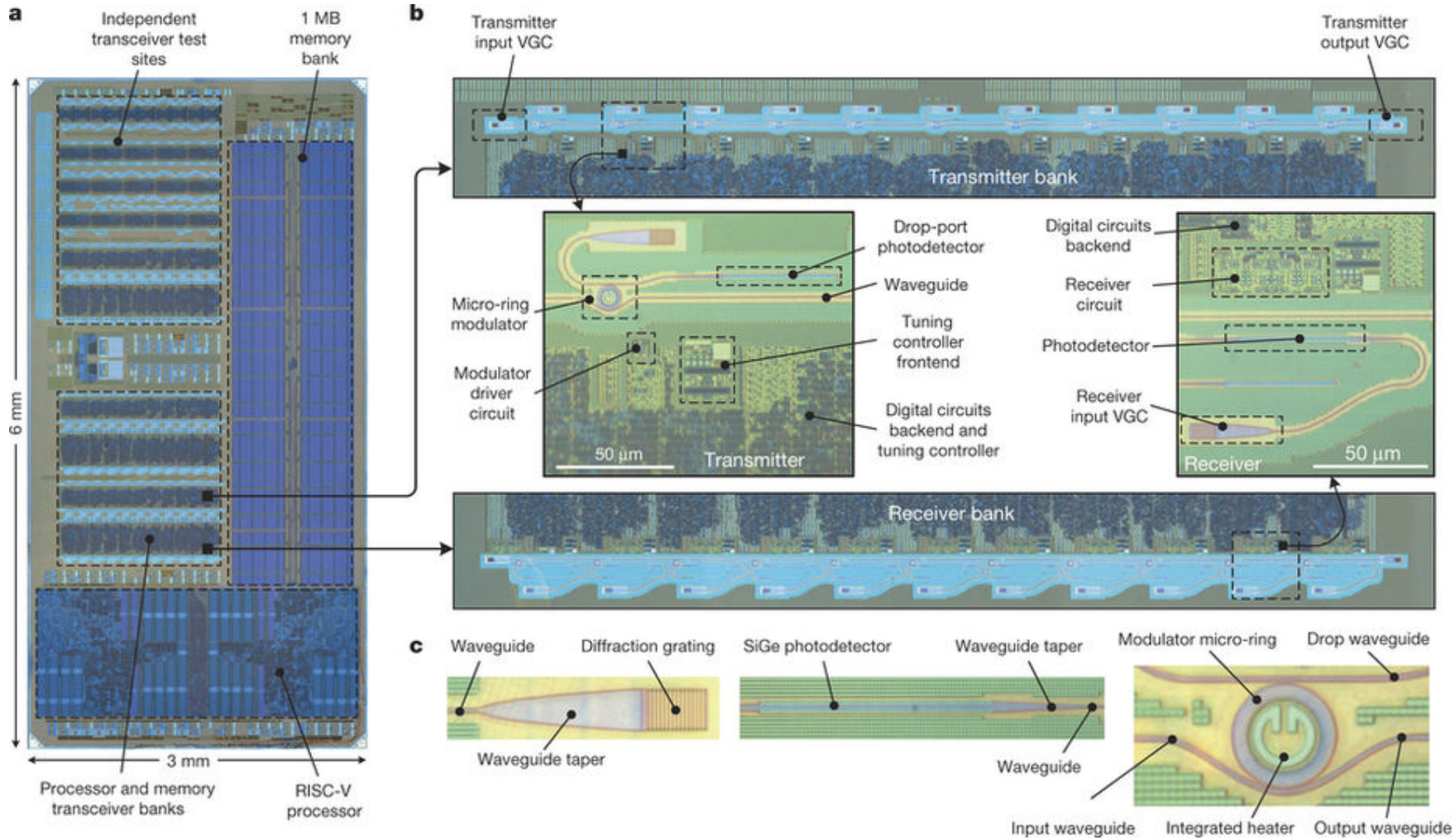


Heterogeneous materials integration challenge:
monolithic, continuous process flow with associated economic advantages

A. Paolella, Harris, IPSR 2016, RF Photonics Chapter

Functional Blocks

3mm x 6mm e-p chip



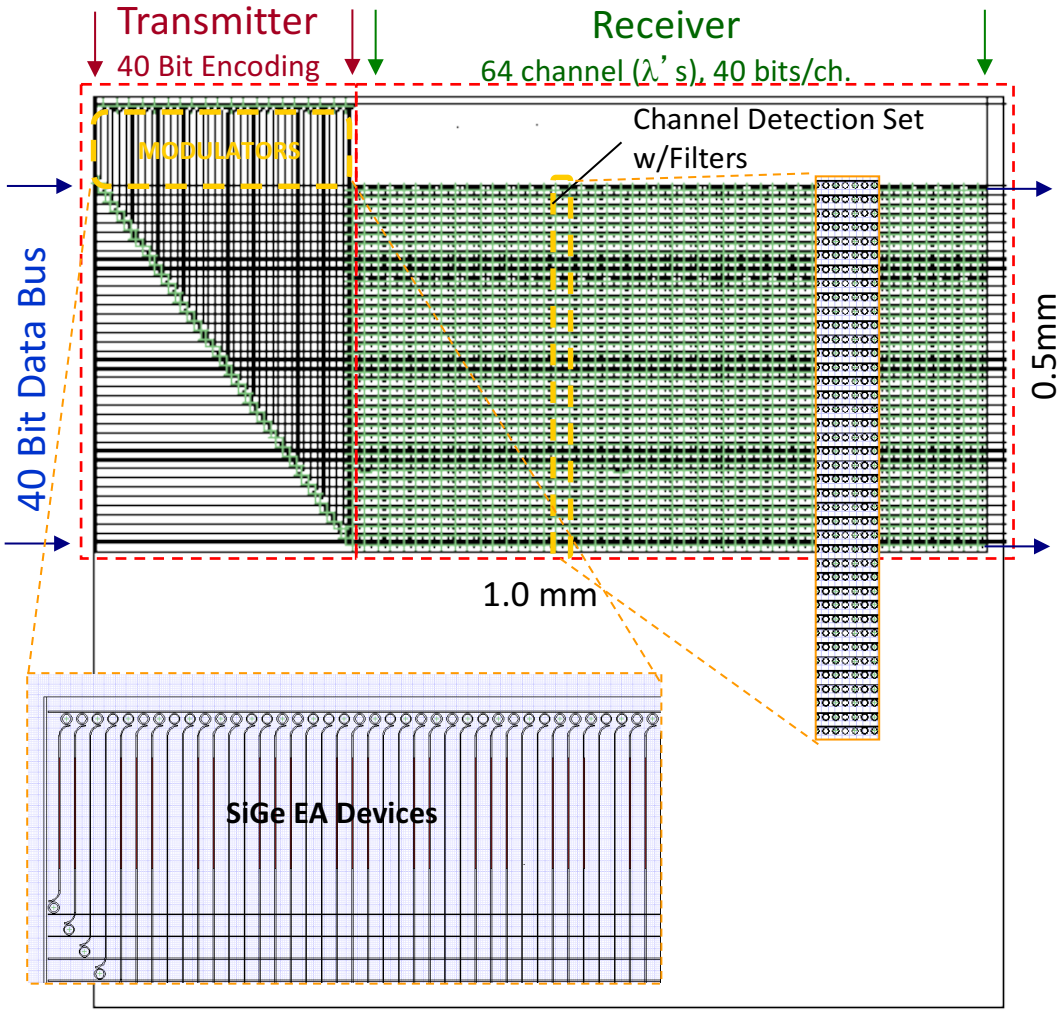
transmitter/receiver banks; coupler, photodetector, ring modulators

electronic–photonic system-on-chip: >70M transistors and 850 photonic components

"Single-chip microprocessor that communicates directly using light", Sun, et.al., Nature, 528 534 (2015).

Technology: WDM Front End

LSI Photonics: I/O for 32 bit Network



Single Tile 1mm² Area of a Multi-Core Processor

64 λ Node Multicore Core WDM Scenario at 1mm² per tile

Single Wavelength per Tile ID

- 64 λ WDM
- Si/SiO_2 HIC waveguide
- 40 wg – 32 data, 8 metadata
- Tile area used: 0.5mm²

Tile Transmitter

- 40 modulators for each core
- Single wavelength for all bit lines
- SiGe EA modulator & driver

Tile Receiver

- 63 ch. (N-1) receiver section per tile
- 40 one bit data lines
- 5um Ring Resonator Filters
- SiGe Detector integrated w/Filters

chip/package/board-level networks driving LSI silicon photonics

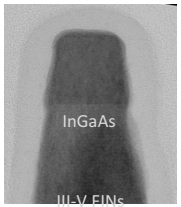
Technology: LSI Scaling ***... Questions?***

Building the Integrated Photonics Manufacturing Ecosystem

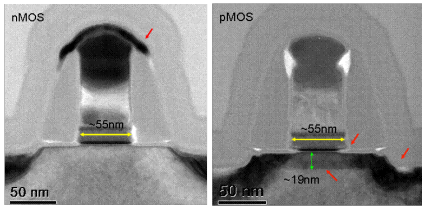
Si Wafer Processing Hub

- Years of proven silicon photonics results
- 300mm tools provide outstanding quality photonics
- 3D stacking w/CMOS
- Partnerships drive continuous revitalization investments

Post S-MLD

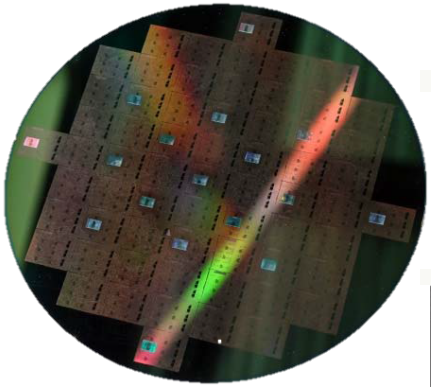


IV-IV 65nm Si CMOS

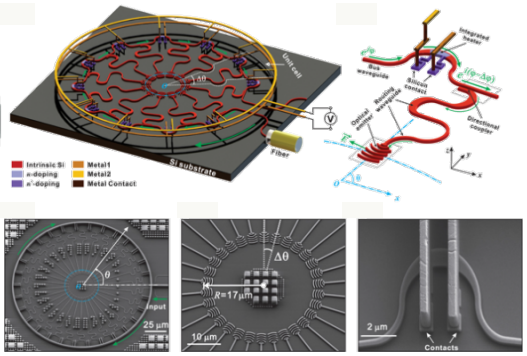


Undamaged III-V FIN

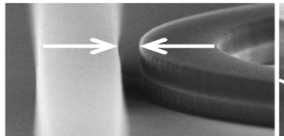
300mm Si Photonics Wafer



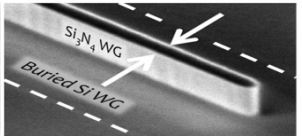
Continuously Tunable Optical Orbital Angular Momentum Generator



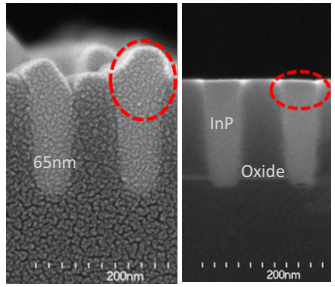
95nm gap in Si



95nm Si_3N_4 Taper on Si Waveguide



Prior | Post CMP

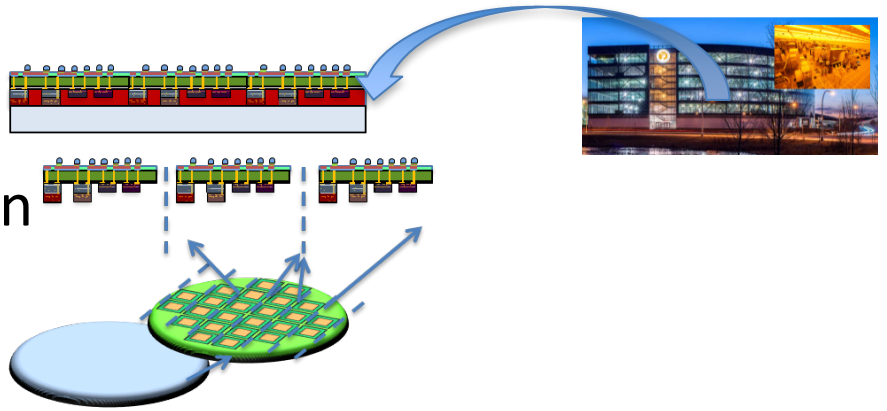


Albany, NY

Manufacturing

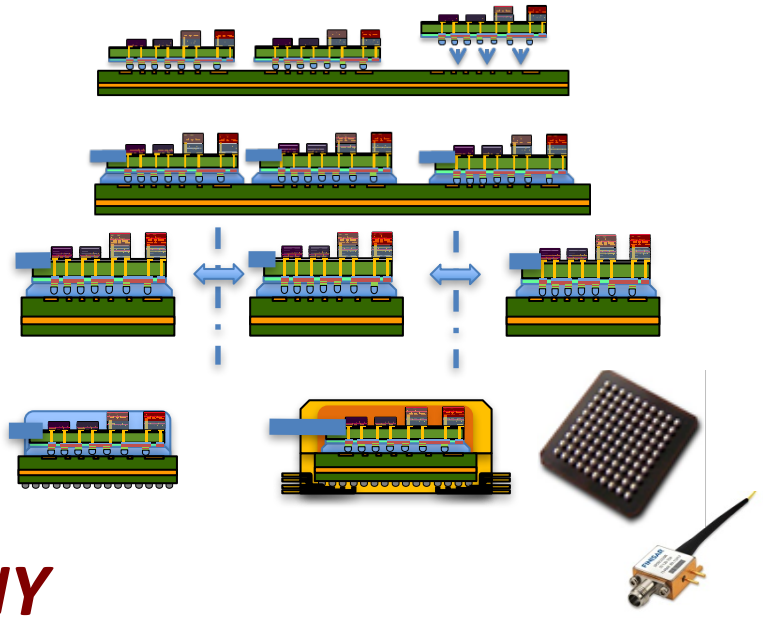
Test Assembly and Packaging Hub

1. *Wafer-scale* photonics packaging
   - First-level interposer metallization
   - De-bond and dicing of wafers



70-80% of the cost of a Si-photonic system is in the package

2. *Chip-scale* test, assembly and packaging
   - Laminate and fiber attach
   - High-speed test and BIST



Rochester, NY

Manufacturing

Workforce and Industry Survey Report

1 Year from now	3 Years from now	5 Years from now
Funnel/vector students in related areas into IP start training from early on in school carrier market appeal of IP to draw interest short courses for broad Ed level (online/pre-recorded) short courses for specialized skills (higher education)	Offer lots of hands-on training to students (MS/PhD level first then BS) heavier marketing of IP appeal offer diversity in skills thoughts--specialty tracks on BS and MS offer IP focus programs: MS; BS--tracks students from early on degree	Have students ready to graduate who have been devoted to IP from the beginning
Establish working MPW model with working EDPA tools to enable R&D ventures in Silicon Photonics	Establish product packaging solutions to target the various markets for optical products	Establish Packaging HVM capability to support volume growth to compete in worldwide markets.
Establish a baseline for full integrated photonics production. Provide initial training to access production runs.	Engage standard bodies for package processes . Successfully scale out PICs for larger volume production.	Broaden HVM applications beyond the datacom sector.

- **Chip fabrication**
  - Ge-epi at 45nm node: compatible thermal budget
  - optical I/O options: v-groove, optical pins
  - hermeticity
  - 300mm challenges: test, C_{PK} and cost
- **Board-level Interconnection**
  - TxRx: pluggable (reliability) vs. surface mount (cost)
  - established solutions in system test
  - system requirement focus: interfaces (connectors)
- **Design at system level vs. chip shrink**
  - chip-package-module-system co-design

45nm is a compelling transition node for Silicon Photonics.
Connectors limit on-board optical interconnection.

Key Technology Needs for 2018

- **Design**
  - robust Design-for-Yield; package simulation
  - functional blocks: RF-OSP, TxRx, WDM e-p front end
- **Monolithic Integration**
  - system requirements for switch and laser integration
- **Assembly**
  - alignment processes, tolerances and associated costs
- **Connectors**
  - Module-PCB and PCB-cable connectors
- **Packaging**
  - optical requirements for embedded package, vertical/edge access; board surface mount; hermeticity
- **Test**
  - Design-for-Test; in-line monitors

Thank You

and Happy Holidays

Acknowledgements

- AIM Photonics Institute members
- IPSR International contributors
- MIT Microphotonics Center members
- iNEMI members
- OSA/OIDA members
- IEEE Photonics Society members
- SPIE Photonics West participants
- Photon Delta and the World Technology Mapping Forum TWGs