SILICON PHOTONICS

Contents

EXECUTIVE SUMMARY

Summary of the State of the Art

In the past 20 years silicon photonics has emerged as a highly attractive technology for Photonic Integrated Circuits (PICs) because it builds directly on the extreme maturity of the silicon nano-electronics world. Thereby it opens a route towards very advanced PICs with very high yield and low cost. More precisely, silicon photonics PICs are being manufactured commercially today in 200 and 300mm CMOS foundries with a nm-level accuracy and reproducibility, unprecedented from a photonics perspective. The basic technology makes use of Silicon-on-Insulator (SOI) wafers, where the silicon layer on top of a buried oxide acts as the core of the waveguides that interconnect the devices on the chip. With silicon being the guiding material for light - and silicon oxide being the cladding - the technology can address applications in the wavelength range between approximately 1 and 4 μm, thereby including the very important fiber-optic spectral bands centered at 1300nm, 1550nm and 1550(+)nm (O, C and L bands, respectively). Silicon photonics has become the technology of choice of more than a dozen, mostly fabless, companies for high data rate transceiver products in datacenters and telecom networks. Collectively, they deploy an estimated multi-million silicon photonics transceivers in the market.

About 20 silicon photonics manufacturing platforms (partly industrial platforms, partly research institute platforms enabling prototyping and low volume manufacturing) have been established by building on existing infrastructure and know how derived from the silicon electronics industry (see Appendix A1). A typical platform allows for the integration of high speed modulators and high speed Ge-detectors at symbol rates in the range of 50 to 100 Gbaud along with advanced passive functions for beam combining/splitting, wavelength-selective functions, polarization selective functions and off-chip coupling. Some platforms allow for additional functions such as integration (monolithic or hybrid) with advanced electronics, integration (heterogeneous or hybrid) of light sources, and sensing-oriented functions (such as microfluidics). Most of the platforms operate like a foundry: they are accessible to any end-user, either in a full-reticle/full-wafer-lot (FRFL) mode or in a cost-sharing Multi-Project-Wafer (MPW) mode, in which an end user can submit designs for part of the reticle and will receive a few dozen processed chips rather than full wafers. The FRFL mode is expensive (several 100K Euro/Dollar) but results in a low cost per chip (of the order of 10 Euro/Dollar per chip) while the MPW mode is more affordable per-design (several 10 K Euro/Dollar), but the per-chip cost is the order of 1000 Euro/Dollar. When scaling to higher volumes (e.g., 1000 wafers) the chip cost can be reduced to below 1 Euro/Dollar per chip, because fixed mask and overhead costs are amortized across the lot. Low cost per chip also benefits when the investment in the foundry infrastructure is already depreciated by or is shared with other users.

Chip foundries make available Process Design Kits (PDKs) to their customers. These PDKs spell out in detail the design rules for the given platform and contain a library of basic components and circuits. The maturity of the silicon photonics PDKs has not reached the level of a CMOS IC foundry. Today, silicon photonics PDKs contain libraries of only very basic building blocks, especially for the MPW-mode of operation. It is imperative that future silicon photonics PDKs contain compact models for components and circuits, with parameters based on validated measurement data, taking into account process variability across wafer and wafer-to-wafer.

SOI-based silicon photonics is limited to a wavelength range of 1 to 4 μm due to the material properties of silicon and silicon oxide. However, research has developed a rich portfolio of options for translation into platforms for commercial use. For the visible and near IR wavelength range, silicon nitride waveguides on a silicon wafer 'handle' have been effective in extending performance at both ends of the spectrum. The silicon photonics platform now provides full functionality from UV to mid IR.

Numerous approaches are being explored for laser integration of the silicon platform: monolithic epitaxial approaches (SiGe, Sn-alloys, III-V), heterogeneous approaches (bonding or transfer printing of III-V on silicon) and hybrid approaches (flip-chip, edge-coupling of chips). At present, only a limited number of specialized fabs offer wafer-scale integration of light sources. The issues of manufacturability, cost and reliability are paramount.

The potential application and market space for silicon photonics is predicated of its combination of performance, yield, reliability and cost. Today's commercial driver is datacom and telecom infrastructure. Consumer markets, such as LIDAR, point-of-care and personalized medicine, medical diagnostics, structural monitoring devices, and devices operating in an IoT context, have the potential to be vastly larger. High performance computation has adopted optical interconnection and quantum computation with silicon photonics is likely to follow when it becomes viable. The aggregate market size will be determined by the performance and manufacturing volume scaling of silicon photonics, both in terms of technical performance and in terms of supply chain readiness.

Silicon Photonics serves a diverse set of markets by providing scalable solutions for optical communication transceivers; LIDAR; physical and biosensors; and quantum computing and artificial intelligence networks. With enhanced process design kits (PDKs) the foundry ecosystem provides a scalable path to higher performance and better reliability through increased process control and high wafer throughput with commercially viable cost targets. Silicon Photonic technology scaling is measured by 3 vectors: process yield (>90% good die with a 6-month design-to-process completion), device integration level (now ~10^4 devices/chip) and performance (speed, power, footprint and cost). The purpose of this Silicon Photonics Chapter of IPSR-I is to plot the timelines for scaling manufacturing yield, photonic circuit integration and system performance for key manufacturing applications. The IPSR-I provides the forum for designers, materials and tool suppliers, fabs and end users to reach consensus on technology timelines and the readiness of solutions to meet the projected requirements. The effectiveness of this document is its role in aligning the manufacturing supply chain to synchronously meet yield, integration and performance requirements.

Summary of the Silicon Photonics Roadmap Sections

Infrastructure Analysis Silicon photonics today is a subset of the $450B silicon IC industry. This industry continues to power the Information Age, and the adoption rate of silicon photonics will be gated by the ability of the CMOS and silicon photonics platforms to mutually adapt to the challenges of performance/cost and electronic-photonic convergence. The silicon photonics platform provides infrastructure supporting prototype development to high-volume manufacturing. Around the world 20+ open-access and 5+ proprietary silicon photonics manufacturing platforms exist. The open-access platforms are accessible to any third-party end-user of the technology. Fabless design companies rely on such open-access platforms for their PIC product development. Transceiver chip cost within the next five

years is projected to reach $0.01/Gbps for a 1000 wafer run on the 300mm silicon platform. High accuracy and high throughput Package and Test limit the necessary cost scaling at the system level.

Manufacturing Equipment A complete silicon photonics process flow requires additional capital expenditure for a standard CMOS electronics fab. Dedicated germanium growth tools are required for the photodetectors and electro-absorption modulators. Laser source integration, whether on chip, in-package or in a remote optical power supply, requires yield standardization from a variety of challenging process flows and dedicated equipment for flip-chip, bonding, transfer printing or metal organic chemical vapor phase epitaxy (MOPVE) of III-V materials. The silicon wafer platform provides a compelling manufacturing advantage. Increasing PIC integration levels and adding materials and device diversity, while maintaining production efficiency and high yield, are the determinants for the attribute timeline tables, as they have guided silicon electronics for the last 3 decades.

Wafers and Epitaxy The silicon photonics platform, as with silicon electronics, is typically built on SOI wafers. Research prototypes have employed bulk wafer substrates with deep trenches for optical isolation from the substrate. Germanium, widely deployed for waveguide-integrated photodetector devices, has a lattice misfit with silicon of about 4.2% and unique, integration-compatible growth strategies are used for wafer-scale germanium growth to achieve low defect density. The most widely used deposition/pattern method is a damascene process flow: oxide deposited on SOI, trench etch to expose silicon waveguide, selective Ge epitaxial growth on silicon-only, followed by CMP planarization of Ge.

Wafer Scale Patterning Silicon Photonics uses 248 nm DUV, 193 nm DUV and 193 nm immersion lithography technologies. These lithography options enable feature sizes of sub-100nm. Generally, silicon PICs employ dry etch processes. F, Cl, and Br-based chemistries are optimized for selectivity, directionality and etch rate to provide the waveguide wall verticality (angle of the sidewall) and sidewall flatness that is required to achieve low optical propagation loss.

PDK and Design Automation Process design kits (PDK) acts as an interface between the designer and the fab. In most cases, the designer has access to the PDK of a fab through design software tools. The silicon photonic PDKs are unique to each foundry. They contain documents providing process-related details (platform cross-section, process variability), performance of the device library components, and a list of design rules.

Quality/Reliability Reliability studies have shown excellent endurance for silicon photonics passive devices. The quality and reliability of waveguide-based passive devices are normally conducted to test their functionality against high optical power density. Active devices show reliable operation under optical, electrical and thermal stress tests.

Environmental technologies The environmental impacts linked to the manufacturing of silicon PICs reflect the material and energy inputs into the manufacturing supply chain, unit processes, use and end of life disposal. As silicon photonics leverages the existing CMOS infrastructure, the environmental impact will likely be managed concurrently with the manufacturing of electronic chips. The introduction of MOCVD III-V gas precursors into the process flow will require specific attention.

Test, Inspection, Measurement (TIM) Manufacturers of test equipment provide commercial systems for wafer-level electrical/optical testing of silicon photonics, with fast alignment and precise

control over the z-position of fibers to compensate for wafer bow, and angular control needed for accurate fiber array coupling for simultaneous multi-channel characterization. Moreover, wafer scale automated testing is available for passive and active photonics circuits involving both optical probing using motorized fiber manipulators, electrical DC probing and RF probing using RF probe manipulators. Automated testing and associated data analytics are key to new product ramp, and Design for Test scribe-line test structures are standard for silicon in-line inspection and test.

Roadmap of Quantified Key Attributes Performance requirement charts are given for commercial deployment with a Manufacturing Readiness Level (MRL) > 7. Performance projections are given at 10-year intervals for Waveguides, Filters and Passive Devices; Photodetectors; Modulators (MZM, Ge EAM, heterogeneous integration); Thermo-optic Phase Shifters; Lasers and Gain Blocks; I/O Couplers & Connectors; and Optical Isolators; and Electronic-Photonic Integration. Attributes with significant externalities and interdependencies outside of the silicon platform are given with more exploratory 5-year intervals in the Gaps and Showstoppers section.

Critical infrastructure Needs The maturation of silicon photonics to fully accommodate the efficiencies of the CMOS process infrastructure will be the focus of the next decade. Manufacturing system integration is the grand challenge. Standardization of materials, design packaging and functional blocks will emerge. Design at the system level with cost, energy, latency and bandwidth density as the prioritized requirements will be the new skill set.

Workforce The technology supply chain supporting the pervasive commercial deployment of silicon photonics begins with the workforce. The worldwide silicon workforce of 350,000 technicians and engineers has little exposure to photonics, and the equally large photonics workforce is unaware of the rigid, efficient infrastructure that underlies its 50% performance/cost learning curve. There is a shortage of skilled experts in the field: manufacturing technicians, design engineers, test engineers, technology developers, PDK developers, application and system integration engineers.

Design Automation The Process Design Kits (PDKs) of most open-access silicon photonics foundries is still relatively limited with respect to their library of building blocks: only basic active and passive components are available and often the degree of technical validation of these components is limited. The availability of accurate compact models can limit the device library. This infrastructure is in stark contrast with the world of electronic design where foundries make available extensive libraries of validated circuits to the designers of their customers.

Design for manufacturability and testability Given the intrinsically analog nature of most photonic circuits it will become increasingly difficult to make designs that are robust against process variations, in particular for LSI photonic circuits. Ensuring a high yield of devices that satisfy system-level specifications will become increasingly more challenging.

Evolution of the platform **A** very rich diversity of impressive, research achievements is emerging to boost the functionality and performance of silicon PICs for an ever-growing range of applications and markets. The platform will be driven by both application pull and by new capabilities.

Key Silicon Photonics Technology Milestones for the next 5, 10, 20 years

Needs 2025

- Silicon photonics manufacturing capability for both low (~10^3) and high (>10^6) chip volume runs.
- Ubiquitous, automated chip design supported by IP license/indemnity infrastructure
- Short cycle times from prototype to commercial manufacturing.
- Manufacturing platforms capable of cross-market applications
- Wafer-level inspection and test; Known Good Die

Needs 2030

- Wafer scale integration of lasers and gain blocks for components and optical power supply: technology decision among hybrid, heterogeneous, monolithic and interposer/package solutions.
- 3D waveguide routing for scaling integration and performance at constant reticle size
- Chip optical interface without fiber attach: surface mount and PCB waveguide traces
- Thermo-optic resiliency for filters, modulators and lasers.

Needs 2040

- High radix matrix switch solution: > 256 x 256
- Monolithic integration of electronics with photonics with co-design for e-ph synergy for high bandwidth density transceivers
- Mutually compatible electrical and optical fanout for ubiquitous in-package optical I/O
- Scaling rules for electrical and optical power distribution for e-ph chip sets

INTRODUCTION

The Information Age has introduced connectivity, control and analysis into most aspects of human existence. A Fourth Industrial Revolution is unfolding with the emergence of High-Performance Computing (HPC), Internet of Things (IOT), smart sensors, big data analytics, cloud computing, Artificial Intelligence (AI), quantum information processing, and Augmented/Virtual Reality (AR/VR) technologies. These technologies will impact the products and operations of a broad range of economic sectors including medicine, agri-food, transportation, construction and energy. The pervasive deployment of new information applications was enabled in the past three decades by the introduction of short product cycle times with advanced manufacturing methods. The Grand Challenge for the next two decades is the continued exponential scaling of functional performance at a rate of 1000x every 10 years within essentially constant cost, energy and space envelopes.

Coordinated advances in hardware, software and system architecture are required. In the case of computing, the end of transistor scaling requires parallel architectures to preserve energy efficiency. Special purpose components and systems, designed-for-function within the envelope constraints, will proliferate. Photonic functionality will migrate from pure communication to repartitioned communication, processing and sensing roles. Today's essential components, such as the optical transceiver, will dissolve into embedded roles in seamless photonic-electronic circuits and systems.

These technology trends require establishment of an effective platform for photonic component integration. Silicon photonics with electronics in its close proximity is the desired end point for the currently perceived chip and module solutions. In the case of computing, a monolithic platform eliminates interfaces that introduce cost, power dissipation and latency. The silicon photonics platform enables scaling by known design utility, and it facilitates faster time to market for manufactured products. Silicon photonics delivers manufacturing yield, throughput and process tool utilization by solving manufacturing problems at a platform level. A silicon photonics platform enables tradeoff analyses among cost, energy and density.

Global trends in system architecture are driving changes that percolate to the chip level. Telecommunication networks, free from copper constrained bandwidth, are migrating back from routed packets to transparent, low overhead circuit switched architectures. Data centers, HPC systems and multicore processor chips are adopting similar network configurations. Network dis-aggregation further drives a platform-based (permanently installed single mode fiber) interconnection infrastructure that facilitates optimization and retrofitting of function (processing, storage, switching).

Silicon photonics manufacturing is enabled by the infrastructure and knowhow of the silicon CMOS electronics world. Today, silicon photonics wafer lots are manufactured almost invariably by using the spare capacity of existing fabs. Thus, silicon photonics chips can be produced with a level of yield and sub-micron accuracy that is unprecedented in the field of photonics. The volumes involved – so far mostly for the fabrication of transceivers – are high from a photonics perspective but low from a CMOS fab perspective. The cost per chip is low from a photonics perspective (because of the enormous re-use factor) but relatively high from an electronics perspective (because of the NRE-cost resulting from the development and maintenance of a photonics process flow and PDK). In the future, two trends will likely emerge. As volumes of silicon photonics products will gear up, we will see dedicated investments in fabs for silicon photonics. In parallel and given the drive towards electronics-photonics co-integration, in particular for computing, we will see the maturity and yield of photonic circuit manufacturing develop

further to be on par with its electronic counterpart so that integration becomes sensible. In the long-term, investments in fabs that serve this need will be made with a mindset of electronics-photonics convergence.

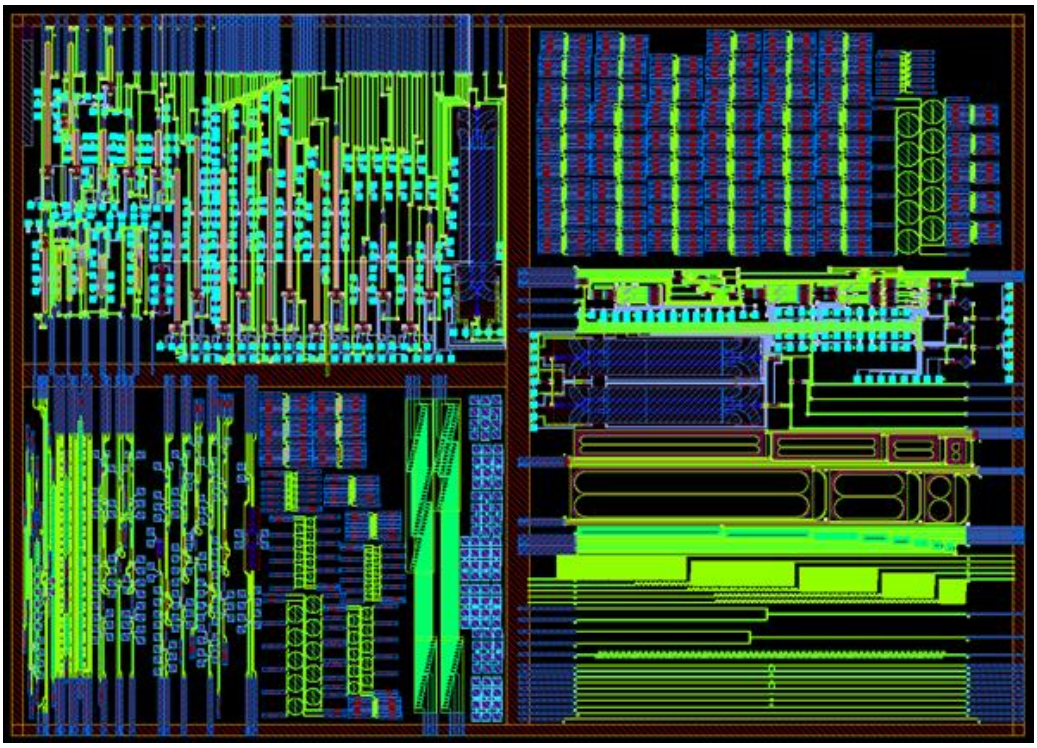

Figure 1: AIM Academy Education Chip: an exemplary silicon photonics PIC design demonstrating a high level of integration density. (Source: AIM Photonics Institute Education Chip)

Smart sensing is becoming ubiquitous over a broad range of applications: automotive, medical, environmental, and structural monitoring. Sensing functions – even very advanced ones – are moving from specialized environments to end-user environments, and in many cases, they will become commodities, with integration into smartphones and tablets. In other cases, they will form the unit cell of large sensing networks, interconnected by RF or optical links, to create an Internet of Things (IOT) chip. Silicon photonics will enable low cost high-volume manufacturing to facilitate widespread deployment of physical and chemical parameter measurement by light. Manufacturing unit volumes for silicon photonic components are projected to be billions per year, far beyond the current millions per year. Today commercial products primarily employ two wavelength ranges: 1550nm for telecom and 1310nm for datacom. Sensing applications, driven by sensitivity and selectivity requirements, will introduce wavelength diversity to the silicon photonics platform. Continued benefits from the economies of scale will introduce design tradeoffs between platform stabilization and optimum performance to meet market performance/cost points.

The silicon photonics platform is diversified at the process level by the material used for the optical guiding layer and the layer thickness of the guiding layer. These choices support a range of applications for telecom, datacom, light-based ranging systems, chemical sensing, and life-science applications.
The rapid momentum in the development of 'silicon photonics' is especially noteworthy based on silicon nitride waveguides. The key asset of silicon nitride (versus silicon) is the capability to address other

wavelength ranges and the potential to drive down waveguide losses even at high optical power. Furthermore, the somewhat lower index contrast of silicon nitride waveguides relaxes the extreme sensitivity of SOI-waveguides concerning the fabrication imperfection at the nanometer level. The roadmap has added a separate chapter describing the Silicon nitride PIC development.
The most mature silicon photonics platform are based on SOI-components for passive and high-speed modulation and epitaxial germanium for detection functions. A lot of current research aims to facilitate materials diversity for the platform, thereby boosting performance and functionality by combining SOI with non-standard materials, either by monolithic, epitaxy-based approaches or by heterogeneous, bonding-based integration approaches. There is an apparent 'conflict' here between the drive for standardization in highly mature and generic platforms that serve many markets, and the drive for new functions that serve specific (but possibly large) markets.

Today, silicon photonics wafer lots are manufactured almost invariably by using the spare capacity of existing IC fabs. By leveraging the tolerances built into the fab processes, silicon photonics chips can be produced with a yield that is unprecedented in the field of photonics. The volumes involved – so far mostly for the fabrication of transceivers – are high from a photonics perspective but low from a CMOS fab perspective. The cost per chip is low from a photonics perspective (because of the enormous re-use factor) but relatively high from an electronics perspective (because of the NRE-cost resulting from the development and maintenance of a photonics process flow and PDK). As the unit volumes of silicon photonics products increase, dedicated investments in fabs for silicon photonics will take place in parallel with a drive towards electronic-photonic co-integration. The dominant long-term trend is platform investment with the mindset of electronic-photonic convergence.

INFRASTRUCTURE ANALYSIS

Silicon photonics today is a subset of the $450B silicon IC industry. This industry continues to power the Information Age. The adoption rate of silicon photonics will be gated by the ability of the CMOS and silicon photonics platforms to mutually adapt to the challenges of performance/cost and electronic-photonic convergence. This section describes the current state of that infrastructure within the requirements of silicon photonics manufacturing. Manufacturing Equipment is evaluated for the unit processes for substrates, epitaxy, lithography, and etch. The current status of Manufacturing Processes, Wafer Materials, Design Automation, Quality and Reliability, Environmental Impact, Test-Inspection-Measurement, Manufacturing Platforms, and Manufacturing cost are summarized and evaluated in the context of expected increases in unit volume production capacity.

MANUFACTURING EQUIPMENT

Silicon photonics requires tighter dimensional tolerances than CMOS technology for acceptable performance of silicon PICs. For example, a variation of 1 nm in waveguide width or height produces 1nm or 2nm spectral shift, respectively, for wavelength selective devices built on the 220 nm SOI platform. This extreme level of dimensional control is achieved by leveraging the toolsets from 200mm or 300mm CMOS infrastructure for PIC manufacturing. The CMOS toolset provides the benefits of (1) unit volume scalability (1-10-100M units/year) with efficiency of scale, (2) reduced cost of $1/mm^2 at even moderate volumes, (3) nanometer-scale dimensional control, (4) reduced test cost with wafer-scale testing equipment, and (5) wafer-scale 3D-Packaging and assembly techniques such as TSVs and solder micro-bumps. For optical datalink applications, the critical dimensions (CD) for silicon photonic PICs are generally achievable with 130 nm - 90 nm CMOS process technology node based on 193nm deep UV

lithography. However, in demanding applications such as advanced optical filters the High Index Contrast (HIC) of sub-micron waveguides demands an accuracy that can only be delivered by a 45 nm or 65 nm CMOS node, with dry or immersion lithography. These most advanced tools for lithography and etch are available only for 300 mm wafers, where the wafer and processing costs are significantly higher than for 200 mm wafers.

Applications for longer wavelengths (MWIR and LWIR) and moderate index contrast such as silicon nitride may have more relaxed line edge roughness requirements but the sensitivity of precision pattern transfer for photonics will continue to require advanced lithography and etching infrastructure for manufacturing yield. Wafer sizes of 100 mm, 150 mm, and 200 mm are competitive at low volume if manufacturing yield is maintained. For the thick SOI platforms, 248 nm and 365 nm lithograph tools sets that process 150mm or 200mm wafer sizes, are sufficient for most communications and sensing platform elements, providing a lower barrier of entry for process cost and capital investment.

The deployment of CMOS processes for silicon photonics introduces certain challenges. For example, silicon is not used for photodetection at telecom/datacom wavelengths. SOI-based silicon photonics relies on low-defect density epitaxial growth of Ge-on-Si for photodetection. A complete silicon photonics process flow requires capital expenditure for dedicated germanium growth for the fabrication of photodetectors. This added capital cost, however, is minimal for a 300 mm fab in comparison to the patterning cost. Today, almost all Silicon Photonics foundries have PIN Ge photodetectors in their PDK. SiGe stressors are already used for the 90nm and lower CMOS nodes. As the industry develops quantum well and quantum dot based SiGe devices for efficiency improvements and additional applications, throughput will become an issue that will require more deposition tools or tools with more chambers.

Addition of III-V tools to the fab, whether for monolithic, heterogeneous or hybrid integration of III-V detector or modulators or lasers, is a more disruptive challenge. Laser source integration requires yield challenging process flows and dedicated equipment for flip-chip bonding, transfer printing or epitaxy of III-V materials.

The silicon CMOS platform has a compelling manufacturing advantage. Increasing PIC integration levels and adding materials and device diversity, while maintaining production efficiency and high yield, is a familiar problem about which the silicon culture has been built.

The discussion in the below sub-sections and the corresponding tables (**Table 1** to **Table 7**) outlines the technology needs for wafers, epitaxy, lithography, etching, and the other key technology modules.

Wafers and Epitaxy

SOI wafers with a 200-250nm thick crystalline silicon layer thickness have a typical layer thickness uniformity of a few nm. The distinguishing feature of photonic SOI substrates is the thick BOX (buried oxide) layer (~ 2µm); ICs employing SOI substrates have BOX layer thicknesses of 50-100nm to maximize thermal transport. Silicon photonics wafers are available in sizes of 100 mm, 150 mm, 200 mm and 300 mm. The most advanced fabs use 300 mm wafers for manufacturing. The Smart-cut process to produce Unibond wafers is currently the favored SOI wafer for PIC manufacturing due to its ability to provide high-quality silicon layers. Thick silicon (> 1µm) SOI technologies for PIC manufacturing mostly

rely on 150mm and 200mm wafers. These wafers have higher thickness variations (typically ~100 nm) which are tolerated by the PIC designs.

Bulk wafer substrates can be employed for monolithic integration of electronic and photonic components. Optical isolation is achieved by etching deep (~ 2µm) trenches, filling with SiO_2 and depositing/patterning the photonic layer locally on the oxide. The layer thickness specifications are identical to the SOI process flow.

Table 1: Technology needs for substrate and epitaxy

Substrate	[unit]	2020	2030	2040	Comments
layer thickness uniformity Si	%	+/- 0.75	+/- 0.5	+/- 0.2	W
layer thickness reproducibility Si	%	1.29	0.75	0.2	W2W
doping concentration uniformity	%	+/- 10	+/- 5	+/- 5	W2W
doping concentration reproducibility	%	+/- 10	+/- 5	+/- 5	W2W
defect density	Number per wafer	50	30	10	For defects larger than 100 nm
strain reproducibility	%	+/- 10	+/- 5	+/- 5	W2W
strain uniformity	%	+/- 10	+/- 5	+/- 5	W

W=WAFER; W2W = WAFER TO WAFER

Silicon photonics relies on direct growth of low defect density (TDD < $10^7 cm^{-2}$) germanium-on-silicon for waveguide-integrated photodetectors. Typically, a Ge buffer layer is deposited at low temperature (~350C) to provide conformal coverage, followed by high temperature (~ 750C) layer deposition. The most widely used deposition/pattern method is a damascene process flow: oxide deposited on SOI, trench etch to expose silicon waveguide, selective Ge epitaxial growth on silicon-only, CMP planarization of Ge for thicknesses >1µm. Defect density is reduced for low area deposition, the oxide junction edge passivation, and the photodetector is self-aligned with the waveguide.

Ge EAM devices are comprised of SiGe alloys or compressive strain to move the Ge absorption edge to < 1550nm. Compositional and strain uniformity are important for EAMs. In order to mitigate the impact of the lower Ge thermal budget, additional improvements are required for optimizing key steps like bakes, cleans, growth temperature, as well as diode implant conditions.

Table 2: Technology needs for the epitaxial growth of Germanium

Epitaxial growth of Germanium	[unit]	2020	2030	2040	Comments
layer thickness uniformity	%	+/- 1.0	+/- 0.5	+/- 0.2	wafer
layer thickness reproducibility	%	1.0	0.75	0.2	wafer
layer composition uniformity	%	+/- 10	+/-5	+/-5	wafer
layer composition reproducibility	%	+/- 1.0	+/- 0.5	+/- 0.5	wafer
doping concentration uniformity	%	+/- 10	+/-5	+/-5	wafer

doping concentration reproducibility	%	+/- 10	+/-5	+/-5	wafer
threading dislocation density*	cm^{-2}	$9x10^6$	$<10^6$	$<5x10^5$	blanket film
threading dislocation density*	cm^{-2}	10^7	$<10^6$	$0 – 5x10^5$	selective
strain reproducibility	%	+/- 0.75	+/- 0.5	+/- 0.2	wafer
strain uniformity	%	< 1.0	< 0.5	<0.3	device

Lithography

CMOS pilot lines, MEMS fabs and industrial fabs use projection-based lithography for silicon PIC manufacturing. Silicon photonics, thin/thick SOI and bulk Si, uses 248 nm DUV, 193 nm DUV and 193 nm immersion lithography technologies. These lithography options enable feature sizes of sub-100nm. As a result, devices such as high-efficiency grating couplers, low-loss directional couplers with small imbalance, and low-loss AWGs with low crosstalk are routinely fabricated with high reproducibility and yield. Innovations and increased complexity in passive devices such as sub-wavelength gratings, contra-directional couplers, and Bragg-gratings may require higher resolution lithography for future silicon PICs. Currently, such devices in research mostly rely on e-beam lithography. Thick SOI technologies employ 365 nm i-line or 248 nm DUV due to their larger CDs in manufacturing.

Table 3: Technology needs for the stepper/scanner lithography

Stepper/scanner Lithography	[unit]	2020	2030	2040
Overlay accuracy	nm (3σ)	30	20	10
Flatness requirements	nm	1000	500	250

Table 4: Technology needs for the e-beam lithography

E-Beam Lithography	[unit]	2020	2030	2040
Overlay accuracy	nm	20	15	10
Required Flatness requirements	µm	0.5	0.2	0.2

Etching

Generally, the manufacturing of silicon PICs uses dry etch processes. F, Cl, and Br-based chemistries are optimized for selectivity, directionality and etch rate to provide the wall verticality and sidewall roughness that is required to achieve low waveguide propagation loss. Techniques such as time-multiplexed etch and passivation cycles, thermal oxidation, double oxidation, hydrogen annealing, and wet chemical treatment have been used to reduce the waveguide surface roughness. The standard silicon etch processes of CMOS toolsets are sufficient in most cases. Thick SOI, deep isolation trenches for optical isolation in bulk Si platforms, and the fabrication of edge couplers in thin SOI platforms require MEMS-like deep etch tools. Etching of other materials used in the manufacturing of silicon PICs such as silicon dioxide, silicon nitride, germanium, and various metals is also required.

Table 5: Technology needs for dry etching (220nm Si: SOI silicon thickness will affect these numbers)

Dry etching	[unit]	2020	2030	2040

side wall roughness	nm	5	3	1
side wall angle	degrees	>85	87	89
etch depth reproducibility (shallow etch)	%	10	5	2
etch depth uniformity (shallow etch)	%	1	0.75	0.5
selective etch masking layers	dependent	dependent	dependent	dependent
minimal linewidth	nm	130/90	65	32
minimal reproducibility	nm	20	10	5
wave guide width uniformity	%	4	2	1
minimum spacing	nm	130	65	32
minimum grating pitch	nm	300	150	75
grating etch step uniformity	%	1	0.75	0.5

Other technology modules

Apart from lithography and etching, a full process flow of silicon PIC manufacturing may include:

- ion implantation to form p-n junctions for modulators or detectors
- thermal annealing for drive in and dopant activation, for reducing the waveguide sidewall roughness or for achieving lower surface roughness polysilicon by recrystallization of amorphous silicon
- deposition of passivation, cladding and dielectric waveguiding materials
- CMP to planarize and reduce the topography of the wafer
- metal deposition for thermal heaters or for ohmic contacts or contact pads
- wafer bonding for 3D-stacking of other materials onto silicon
- dicing/cleaving for chip level testing of silicon PICs.
- thin film dielectric/nitride deposition for protective layers, cladding layers, AR coatings, or additional waveguide layers
- cleans: (When metal or germanium is deposited and not properly cleaned, the metal residue can give very high loss)

undercut for thermal isolation

Table 6: Technology needs for various other technology modules

Thermal budget	**[unit]**	**2020**	**2030**	**2040**
a-Si to poly-Si	[C]	600	600	600
Dopant implant activation	[C]	900	800	700
Planarization	**[unit]**	**2020**	**2030**	**2040**
Required flatness	nm	20	10	5
Uniformity	%	2	1	0.5

Selectivity	dilution/pH/slurry	interdependent	interdependent	interdependent
Dicing / cleaving	**[unit]**	**2020**	**2030**	**2040**
Position accuracy	[µm]	50	20	10
Metal deposition	**[unit]**	**2020**	**2030**	**2040**
Thermal budget	[C]	450	400	350
Wafer bonding	**[unit]**	**2020**	**2030**	**2040**
Thermal budget	[C]	300	250	200

MANUFACTURING PROCESSES

A schematic view of the FEOL process sequence to fabricate photonic devices is shown in **Figure 3** The major features reflect the layer-by-layer process flow determined by the lithography mask set and PDK.

(i) Etch levels for the silicon waveguides are specific to strip, deep etch rib, or shallow etch rib waveguides. The etch levels also define the grating couplers for optical IO. The typical width of an SOI waveguide is defined by the single-mode condition of the waveguide. For 220 nm SOI, this width is typically 400 to 500 nm. Narrow waveguide tips (inverted tapers) increase the mode size for edge couplers. A typical width of the tapered end is 100 nm or less. Rib waveguides have a typical width of 650 nm at 220 nm thickness. The thick SOI platforms have only rib waveguides for single mode operation. Passive devices such as MMIs, AWGs, ring resonators, waveguides and grating couplers for IO are defined by using the three etch levels in SOI.

(ii) Modulators require P-doping and N-doping in and around the rib waveguides. High-speed Si modulators employ the plasma dispersion effect and carrier depletion. For electrical contacting, P+, P++, N+, and N++ dopings are also available. The silicide module is similar to that used in a conventional CMOS process. Any kind of standard silicide material, such as $TiSi_2$, $CoSi_2$ or NiSi, can be used for the photonic platform since no critical-sized patterns require silicide. The silicide module reduces the active device contact resistance for doped silicon. Thermo-optic phase shifters are implemented with silicide metal or with doped waveguides for joule heating.

(iii) High-speed photodiodes, electro-absorption modulators and lasers in silicon photonics are built with epitaxially grown germanium. Lateral and vertical PIN and lateral MSM configurations for photodiodes are possible. The silicon photonics platform provides routes for integrating light sources at the wafer level. These approaches include wafer-level flip-chip-based integration, wafer-level epi-bonding-based integration, wafer-level transfer-printing-based integration, and monolithically integrated III-V and Ge(Sn) lasers.

(iv) Contact and interconnect metallization.

WAFER MATERIALS

The wafer substrate material and the photonic integration architecture define the manufacturing platform and manufacturing capacity. Two silicon wafer platforms are used today: SOI and bulk Si. The bulk wafer platform provides potentially lower cost and more efficient electronic-photonic co-integration. However, thick 2 micron dielectric (SiO_2 or air) clad isolation layers must be placed under the waveguide transmission lines. The waveguides are comprised of deposited amorphous or polycrystalline materials

(Si or SiN). The SOI platform, with typically a 2 micron buried oxide, provides global isolation for optical waveguides from the handle silicon wafer. The bus waveguides are typically single crystal silicon. Both Si wafer platforms are used in foundry-level production with standard CMOS IC process tools on 200mm and 300mm wafer diameter platforms. For high volume production, > 1 million chips, the silicon wafer provides the most readily available platform capable of the line and die yield required for high volume manufacturing. **Figure 2** shows the three most prominent silicon photonic wafer platforms: thin SOI, thick SOI and bulk silicon.

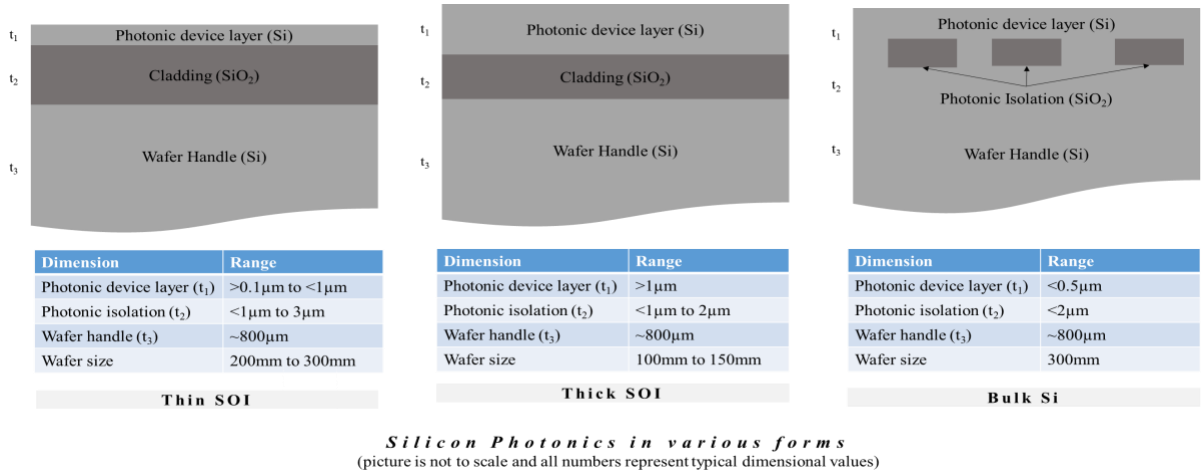

Figure 2: Silicon photonics exists in various forms. Thin SOI is the most prominent form of silicon photonics.

PDK AND DESIGN AUTOMATION

Process design kits (PDK) acts as an interface between the designer and the fab. The silicon photonic PDKs are unique to each foundry, and PIC designers have access to the PDKs. They contain documents providing process-related details (platform cross-section, process variability, etc.), performance of the device library components, and a list of design rules. The component library provided by the PDK has validated fixed-cell building blocks to ease the layout of complex circuits containing 100s or even 1000s of building blocks. Major design software companies are investing to implement Photonic Design Automation (PDA), Electronic-Photonic Design Automation (EPDA) and the implementation of a unified electronic-photonic design flow.

Table 7: Current status of PDK and design automation (PDKs on a manufacturing line are released with compact models, process corner corrections, stochastic models, etc.); example 90 nm GF tech node. (up to 35 Gbps).

Current status of PDK & Design Automation		**Status**
PDKs	Compact models	< 2025 (exist today)
	Corner models	> 2025
	Stochastic models	> 2025 (exist today)
	Component library	Exist today
	PCells	Exist today

	Design rule checks (DRC) – for manhattanized patterns (exist today), the freeform or curvilinear designs are still being developed (soon to be deployed).	Exist today
PDA	Layout-vs-schematic (LVS)	Exist today
	Schematic-drive-layout (SDL)	Exist today
EPDA	Electronic-photonic co-design	> 2025
	Unified electronic-photonic design flow	> 2025

See the EPDA chapter for a more detailed roadmap on this topic.

QUALITY/RELIABILITY

The quality and reliability challenges associated with silicon photonics are addressed at several levels.

- at the level of device designers: techniques to minimize the effect of process variation and thermal fluctuation are incorporated in the device design
- at the level of system designers: active tuning techniques (such as thermal tuning) are used to compensate for the device performance degradation due to process variation or chip thermal variations
- by using a reliability-aware design flow to ensure quality and reliability at the device and system level simultaneously
- reliability of actives (i.e. lasers) and reliability of packaged modules (i.e. fiber attach solutions) – these two factors are the most dominant in the reliability of silicon photonics products.

The quality and reliability matrix for silicon photonics can consist of four parts:

1. Discrete device life-time prediction
2. Full electrical stressing of a bare die without laser
3. Full optical and electrical stressing of the die with a laser
4. The integrity of laser attachment

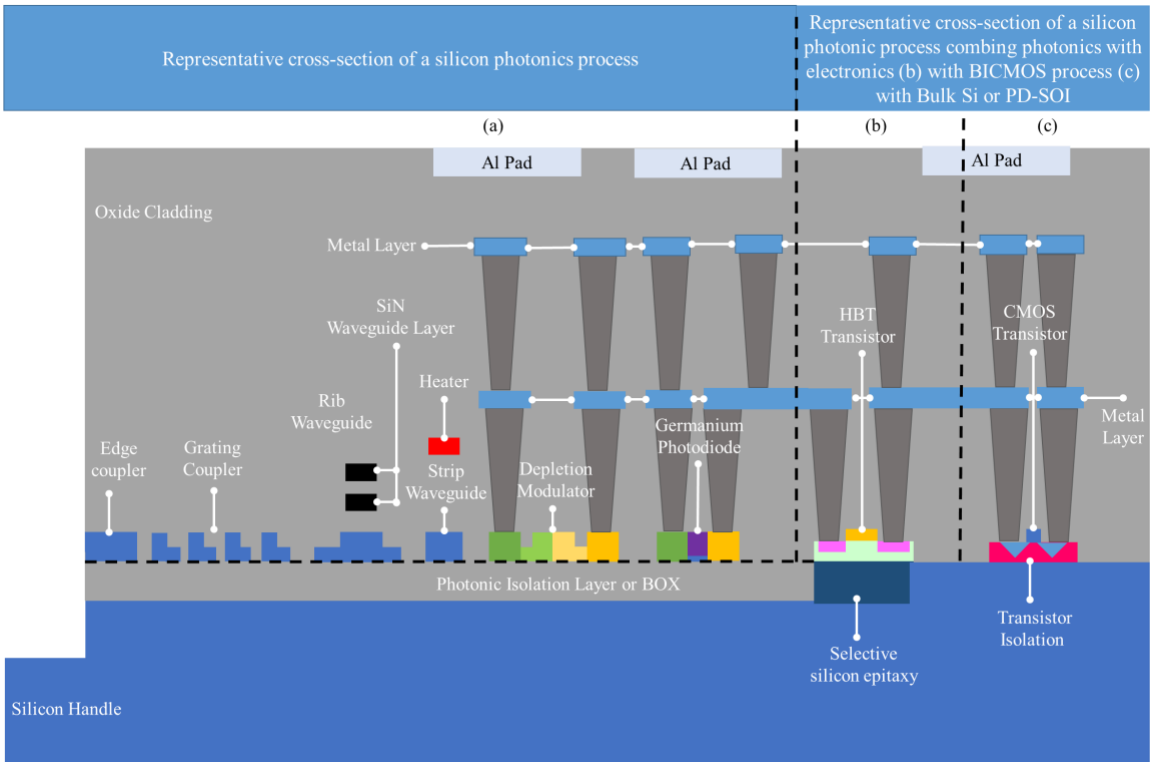

Figure 3: The silicon photonics wafer platforms providing photonic functionalities with or without monolithic integration with electronics. The wafer platforms offer either (a) only, (a)+(b) only or (a)+(c) only.

Experimental reliability studies have shown excellent endurance for silicon photonics passive devices. The quality and reliability of waveguide-based passive devices are normally conducted to test their functionality against high optical power density. Active devices also show reliable operation under optical, electrical and thermal stress tests. Typical silicon photonics Ge PDs and depletion modulators have negligible wear-out failures of below 1 Failure in Time (FIT). Similarly, reliability testing integrated heaters have shown a lifetime of >10 years. As a result of the high intrinsic reliability offered by silicon photonics building blocks, it is estimated that silicon photonics transceiver modules can have over 10 billion failure-free operating hours, which corresponds to a failure rate below 0.1 FIT. MOB-based and flip-chip-based lasers where the III-V die is hybrid-attached to silicon with eutectic solder has proven reliable to Telcordia GR468 standards.

ENVIRONMENT, HEALTH AND SAFETY

The environmental impacts linked to the manufacturing of silicon PICs depend on the material and energy inputs into the manufacturing supply chain, unit processes, use and end of life disposal. As silicon photonics leverages the existing CMOS infrastructure, the environmental impact is not tremendously different from the manufacturing of CMOS electronics chips. Silicon fabs and foundries have adopted best practices to ensure minimal environmental impact. Fabs use materials flow analysis, which utilizes process material input/output data to characterize the use and emissions of materials within and between processes, to identify the scale of environmental impacts and determine the directions for improvement. This material analysis is typically used to perform the life cycle assessment of a product.

Using CMOS foundries for silicon photonics manufacturing can introduce significant, unsolved environmental and contamination challenges for III-V materials integration. MOCVD deposition processes to integrate materials such as ferroelectrics and arsenic containing III-Vs are not covered in fab standard procedures. To overcome the toxic effects related to the use of MOCVD precursors, the industry has developed equipment with computer-controlled gas and chemical delivery systems, toxic and carrier gas sniffing sensors with parts-per-billion sensitivity. All tools and processes, patterning (lithography and etch), cleans and thermal conditions are EHS and tool capability concerns. The timeline and investment for adapting CMOS manufacturing lines to III-V materials needs is undetermined, at present. In the interim, retrofit or III-V last BEOL strategies are likely to be implemented.

TEST, INSPECTION, MEASUREMENT (TIM)

Manufacturers of test equipment provide commercial systems for wafer-level electrical/optical testing of silicon photonics, with fast alignment and precise control over the z-position of fibers to compensate for wafer bow, and angular control needed for accurate fiber array coupling for simultaneous multi-channel characterization. Moreover, wafer scale automated testing is available for passive and active photonics circuits involving both optical probing using motorized fiber manipulators, electrical DC probing and RF probing using RF probe manipulators. The fiber manipulators allow the measurement of any combination of optical and electrical ports within the photonic circuits. For passive photonic devices (such as fiber-grating couplers, waveguides, and filters), the optical transmission spectrum can be measured. For active devices (such as photodiodes and modulators), electrical (at DC and RF frequencies) and electro-optical parameters can be measured. The wafer-scale automated electro-optical testbeds provide:

- efficient coupling of light from or to an optical fiber with minimum coupling variability by using precise alignment, and by compensating the topography of the chuck that holds the wafer during testing
- minimization of unwanted fluctuations from polarization changes, temperature changes and insertion loss changes enabling high quality, repeatable, reproducible and consistent data across multiple wafers

Standard Scribe-line Test Structures need to be developed to facilitate automation and design-for-test. These Test Structures should mimic all properties and performance required from the components, including reliability.

Testing operates in various optical bands (such as O-band, C-band, L-band) and from DC to very high frequencies (>50GHz). Advanced modulation formats (PAM4, QPSK, PDM-QPSK) are implemented. Test equipment that can measure up to 110 GHz is available (PNA/LCA/ 2-port, 4-port). Automated test equipment to measure beyond 110 GHz will be required for 2030.

MANUFACTURING PLATFORMS

The silicon photonics platform provides an infrastructure supporting prototype development to high-volume manufacturing. Around the world, 20+ open-access and 5+ proprietary silicon photonics manufacturing platforms exist, almost all of which build on existing infrastructure from the silicon electronics world. The open-access platforms are accessible to any third-party end-user of the technology. Fabless design companies rely on such open-access platforms for their PIC product development. The open-access platforms are either industrial platforms capable of high-volume manufacturing or research

institute platforms enabling prototyping and low volume manufacturing. Infrastructure for silicon photonics Multi-Project-Wafer (MPW) runs well-established in many of these manufacturing platforms.

MPW-services have also emerged from a variety of rapid-prototyping services. The rapid-prototyping platforms reduce the time from prototype development to high-volume manufacturing while ensuring higher process flexibility to lower the threshold for R&D. In the year 2020, 50+ MPW runs, which can be accessed directly at the fab or via a technology broker, are being offered. More and more platforms offer engineering runs for low volume manufacturing. The industrial platforms support the high-volume manufacturing indigenously, whereas the R&D fabs provide routes to high-volume manufacturing via their partner industrial fabs. **Table A1** in the Appendix section provides information on the capabilities of a selected list of these fabrication platforms.

MANUFACTURING COST

Figure 4 depicts the cost competitiveness of silicon photonics resulting from leveraging the existing CMOS infrastructure for PIC manufacturing. The graph shows the cost/mm^2 for PICs manufactured in a CMOS fab that is close to being fully loaded with CMOS electronics manufacturing. Data for the graph is obtained from various fabs providing a full process flow for prototyping and/or manufacturing of silicon PICs. The cost estimates include the specific capital overheads to set up dedicated processes for germanium growth, which is required to fabricate photodetectors in a CMOS fab. The cost curve does not include the packaging of silicon PICs. It is shown that silicon photonics becomes cost competitive for very modest volumes of manufacturing. For example, for 10 200 mm wafers, each mm^2 of chip area costs < $1.

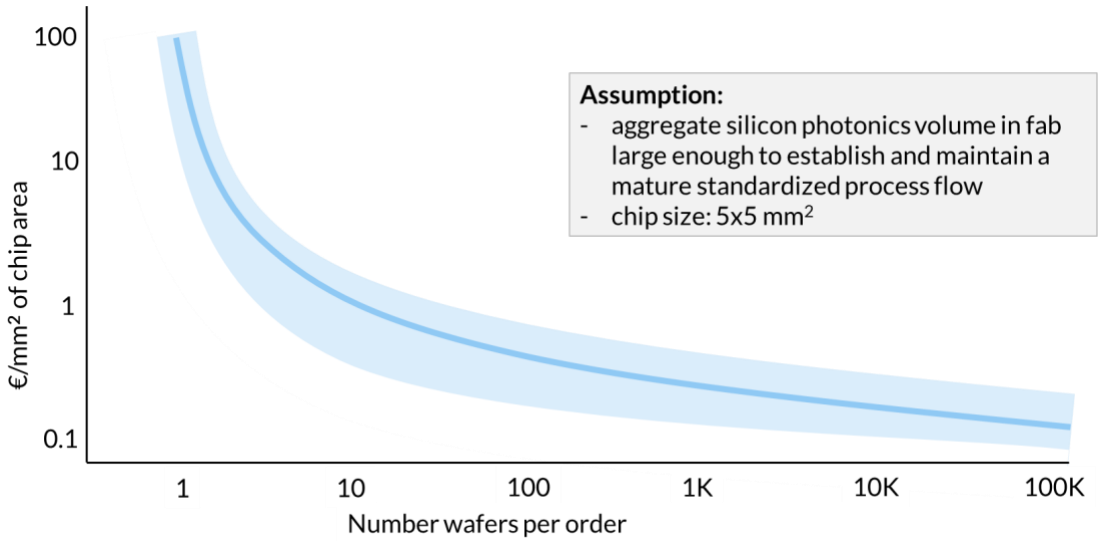

Figure 4: Price per unit mm^2 for a silicon photonics chip manufactured in a fully loaded CMOS fab with a well-established silicon photonics platform. Data are collected by ePIXfab—The European Silicon Photonics Alliance (http://epixfab.eu) from the R&D fabs and commercial fabs.

ROADMAP OF QUANTIFIED KEY ATTRIBUTES

The following sections tabulate the key performance values for the silicon photonics device building blocks. The values represent **projected performance for late stage development and commercial**

deployment with a Manufacturing Readiness Level (MRL) of 7 or greater. For enabling technologies a TRL of 6 means that the technology has been demonstrated in an industrially relevant environment.

WAVEGUIDES, FILTERS AND PASSIVE DEVICES

The silicon-on-insulator platform is uniquely capable of delivering high transparency and high index contrast in the 1200-3500nm wavelength range. This range is ultimately constrained by the transparency of both the core (Si) and the cladding (SiO_2). The use of other materials, such as silicon nitride, replacing silicon or complementing it, enlarges this range. **Table 8** lists key performance attributes of passive waveguides in silicon photonics platforms.

Table 8: Waveguides	[unit]	2020	2025	2030	2035	2040
Waveguide loss	dB/cm	0.35	0.1	0.05	0.001	0.001
Effective index		1.8 - 4	1.8 - 4	1.8 - 4	1.8 - 4	1.8 - 4
Temperature stability (eg ring resonator)	pm/^{o}K	25	10	1	0.5	0.1
Power	mW	30mW	50mW	100mW	200mW	500mW
Dimensional uniformity	nm	3nm	1nm	0.7nm	0.5nm	0.3nm
Material System	Core /Clad	Si, SiNx /SiO_2	Si, SiNx, Ge, multilayer	multilayer	multilayer	multilayer

A wavelength selective filter is a device that can separate individual wavelengths from a waveguide on which multiple wavelengths are propagating. The same device can be used to add wavelengths propagating on different waveguides to a single waveguide. Such filtering devices are useful for optical communications and for applications such as optical spectroscopy.
In optical communications, optical filters are used to multiplex (MUX/DMUX) Wavelength Division Multiplexed (WDM) signals. Scaling interconnection to the highest bandwidth density will necessarily utilize DWDM of > 100 channels/waveguide. The high index contrast provided by silicon photonics leads to a small footprint MUX devices. **Table 9** lists key performance attributes for typical filters or demultiplexers (assuming **no active control**).

Table 9: Filters	[unit]	2020	2025	2030	2035	2040
Crosstalk	dB	30	35	40	45	50
Loss	dB	2	1	0.5	0.2	0.1
Channel uniformity	dB	2	1	0.5	0.2	0.1
Center frequency accuracy	GHz	250	100	50	25	10

PHOTODETECTORS

Materials selection for integrated waveguides is based on the following parameters: material absorption, device dark current and circuit process integration. Germanium-on-Si growth, without a thick graded buffer layer, and dislocation-free Ge in selective area epitaxy, are essential to waveguide-integrated optical devices. Ge-on-Si growth produces a built-in biaxial tensile strain in the Ge that red-shifts the absorption edge to beyond 1600 nm. This extended response is beneficial for detection of C+L bands (wavelength channels allocated for standard wavelength division multiplexed communication [C-band] and extended longer wavelength communication [L-band]) of optical fiber communication. Selective area epitaxy with SiO_2 masking allows submicron wide Ge stripes to be directly integrated on the waveguide. For an optical layer in the BEOL interconnect stack, Ge on a non-crystalline substrate such as SiO_2 or amorphous Si has been demonstrated in research using polycrystalline Ge melting/solidification on SiO_2 and Ge deposition on amorphous Si seed layers. **Table 10** shows the key performance timeline of integrated detectors.

Table 10: Photodetectors	[unit]	**2020**	2025	2030	2035	2040
Absorption	α (cm^{-1})	10^3	10^4	10^4	10^4	10^4
Dark Current	I (nA)	0.2	0.1	0.1	0.1	0.1
Responsivity (p-i-n)	R (A/W)	1	1.1	1.1	1.1	1.1
Bandwidth (p-i-n)	B (GHz)	67	100	150	200	200
Gain x Bandwidth (APD)	GB (GHz)	300	400	500	600	600
Guided Power*	mW	30mW	100mW	100mW	100mW	100mW

*with multiple detectors

MODULATORS

The materials selection for integrated waveguides is based on the following parameters: electro-optic coefficient; insertion loss; extinction ratio; spectral range and process integration.

High-speed Silicon modulators The most widely deployed device is the silicon MZI modulator, because it uses standard junction or MOS process technology to produce devices that modulate the silicon refractive index through the free carrier plasma effect. These devices are capable of OOK and QPSK modulation formats. Si ring resonators offer high bandwidth density and low energy/bit. Thermal control of the silicon ring modulators is employed to stabilize the operation and to precisely tune the modulation wavelength with an added energy/bit penalty that decreases with increasing data rate.

High-speed Germanium modulators The Franz-Keldysh (FK) GeSi electro-absorption modulator (EAM) has been demonstrated for operation at λ =1550 nm. The dilute alloying of Ge with Si moves the absorption edge of as-grown, tensile-strained SiGe to 1550 nm. The FK EA modulator provide the lowest energy/bit performance because of its reverse bias field-only operation. The major issue in device design is the reduction of the operating voltage to CMOS power supply levels of <1V. Compressive-strained Ge-based EAMs for wavelengths shorter than 1550 nm have been demonstrated for potential datacom

applications. Ge/Si quantum well structures exhibit a strong QCSE (Quantum Confined Stark Effect) with potential for lower voltage operation.

New materials Research demonstrations based on heterogeneous integration of new materials include $LiNbO_3$, $BaTiO_3$, $PbZrTiO_3$, organic materials (see polymer TWG) and 2D materials (e.g. graphene).

Table 11, **Table 12**, and **Table 13** describe the performance timeline for high-speed phase modulators, high-speed amplitude modulators, and low-speed modulators respectively.

Table 11: High-speed Phase Modulator	[unit]	2020	2025	2030	2035	2040
Symbol Rate	Gbaud	50	100	400	800	>800
Figure of Merit	V.cm	0.3	0.1	0.05	0.025	0.01
Intensity variation for π phase shift	dB	2	1	0.25	0	0
Materials	-	Silicon	Silicon with new materials	Silicon with new materials	Silicon with new materials	Silicon with new materials

Table 12: High-speed Amplitude Modulator	[unit]	2020	2025	2030	2035	2040
Symbol Rate	Gbaud	50+	100	400	800	>800
Figure of Merit	ER/IL	1	2	4	6	8
Device	-	FKE	FKE, QCSE	FKE, QCSE	FKE, QCSE	FKE, QCSE

Thermal phase shifter In silicon photonics, phase modulation using the thermo-optic effect is used widely for low-speed applications. It has the advantage of simple and low-cost processing and small footprint devices. This is achieved by using Joule heating by either doped waveguides heaters or metal heaters. A typical figure-of-merit for such modulators is the product of electrical power needed for a phase shift and the switching speed. Typically, such modulators consume few tens of mW (down to 1 mW with heat isolation undercuts) of electrical power and have microseconds of switching speed in thick SOI and sub-micron SOI. Such low-speed heaters are instrumental to demonstrate programmable, re-configurable and tunable silicon photonics PICs.

Table 13: Low-speed Modulator/Switch	[unit]	2020	2025	2030	2035	2040
Power: π-phase shift	mW	10	5	2	1	0.5
Loss	dB	0.05	0.02	0.01	0.01	0.01
Bandwidth-power product	MHz.mW	1	0.5	0.3	0.2	0.1

LASERS, GAIN BLOCKS AND OPTICAL SWITCHES

Hybrid and heterogeneously integrated light sources Most applications of PICs require a light source with either a clean optical carrier (laser) or broadband light. III-V materials have for decades been the best performing light source technology. To bring III-V and SOI-based silicon photonics together, a variety of approaches are being pursued. **Figure A2** presents evaluation criteria for III-V on Si hybrid integration methods. The ultimate manufacturing solution is to monolithically integrate a III-V laser source on SOI with high-quality epitaxial growth. The main challenges for this solution are 1) the lattice mismatch between III-V and SOI, 2) the incompatibility of the growth temperature with SOI back-end-of-line and 3) the thermal expansion coefficient differences between the III-V material and SOI. Research demonstrations of monolithically integrated lasers comprised of GaSb, InP, InAs/GaAs or GeSn alloys have been shown for NIR and mid-IR wavelengths.

Hybrid integration and bonding of III-V on SOI are established routes to integrate lasers on patterned silicon photonics wafers. The bonding can be done using direct molecular adhesion or using an intermediate adhesive layer. To preserve the advantage of using CMOS technology on large wafers, it is important to carry out the integration on a wafer scale. New technologies such as micro-transfer-printing allow for transfer of multiple pre-processed lasers simultaneously on a processed silicon photonic wafer. This approach combines the advantages of flip-chip integration and wafer bonding. **Table 14** presents the pros and cons of the different technologies.

Table 14: Pros and cons for various laser integration techniques

Technique (Silicon platform)	Flip-chip	Epi-bonding	Micro-transfer-printing	III-V epitaxy on Si
Efficiency of III-V area usage	+/-	-	+	+
Scaling to volume	+/-	+	+	+
Alignment method	+/-	+	+/-	+
Pre-testing / burn-in	+	-	+/-	+

Switches. For large optical matrix switches, ubiquitous gain block integration within Mach-Zehnder arrays is essential for scaling port count. The device design tradeoff between optically pumped waveguide amplifiers and semiconductor optical amplifiers will be determined by performance: noise figure, footprint and gain/cm.

When single mode chip-to-chip coupling becomes cost effective, regulated wall plug light sources may be architecturally favored for applications such as data centers where photons are everywhere and light source stability is critical. This optical power supply architecture would be a major advance in flattening distributed systems by eliminating tiers in the interconnection hierarchy.

The design rules for laser and gain block integration are shown in **Table 15**.

Table 15: Laser, Gain Block	[unit]	2020	2025	2030	2035	2040
Coupled Output Power	mW	20	35	50	100	200
Gain	dB	15	20	25	30	30

I/O COUPLERS & CONNECTORS

The optical chip interface to the outside world is most often to single-mode fiber. The classical approach is to couple to edges (cleaved or etched facets) of the chip. With the advent of sub-micron silicon waveguides, the technique of grating couplers has become an attractive proposition: the high index contrast makes it possible to engineer gratings with a high coupling efficiency and a relatively large optical bandwidth. With grating couplers, light can be coupled from the surface of the chip, enabling wafer level testing of components before dicing into individual chips.

The design of edge couplers employs narrowing the waveguide tip and covering it with an low index clad layer to achieve an increase in the mode field diameter and index matching with optical fiber. For thick SOI platforms, edge coupling is prevalent. A good match between the mode-field diameter of the rib waveguide in thick SOI and an appropriate lensed fiber results in broadband coupling with low back-reflection and high efficiency. For out-of-plane vertical coupling, mirrors are used in thick SOI platforms. **Table 16** and **Table 17** show the key performance timeline of grating and edge-fired I/O couplers.

Table 16: I/O Coupler Gratings	[unit]	2020	2025	2030	2035	2040
Bandwidth	nm	75	100	125	150	150
Loss	dB	0.8	0.4	0.2	0.1	0.1
Wavelength Accuracy	nm	5	2.5	1	0.1	0.1
PDL	dB	0.3	0.2	0.1	0.1	0.1

Table 17: I/O Coupler Edge-fired	[unit]	2020	2025	2030	2035	2040
Bandwidth	nm	300	400	500	800	1000
Loss	dB	1	0.5	0.2	0.1	0.1
PDL	dB	0.5	0.3	0.2	0.1	0.1

ISOLATORS

The materials selection rules for integrated optical isolators are based on the following parameters: transparency, magneto-optic coefficient, insertion loss and spectral range. Non-reciprocal photonic devices, including optical isolators and circulators, are indispensible components in optical

communication systems. However, the integration of such devices on semiconductor platforms has been challenging because of material incompatibilities between semiconductors and magneto-optical materials that necessitate wafer bonding, and because of the large footprint of isolator designs. Monolithically integrated magneto-optical isolators on silicon are fabricated using a non-reciprocal, optical resonators. This monolithically integrated non-reciprocal optical resonator may serve as a fundamental building block in a variety of ultracompact silicon photonic devices including optical isolators and circulators, enabling future low-cost, large-scale integration. Magneto-optical garnets used in discrete nonreciprocal photonic devices show large lattice and thermal mismatch with semiconductor substrates, making it difficult to achieve monolithic integration of garnets with phase purity, high Faraday rotation and low transmission loss. The only experimentally demonstrated optical isolators on silicon employ Ce-doped yttrium iron garnet films on an SOI Mach–Zehnder or ring resonator structure. Compared to the hybrid solution, on-chip monolithic integration of non-reciprocal photonic devices offers high throughput, high yield, low cost and large scale. **Table 18** shows the key performance timeline of optical isolators.

Table 18: Optical Isolation	[unit]	current	2025	2030	2035	2040
Spectral Range	nm	NA	50	75	100	200
Insertion Loss	dB	NA	3	2	1	0.5
Isolation	dB	NA	10	20	25	30

ELECTRONIC-PHOTONIC INTEGRATION

Silicon photonics is a platform capable of monolithic integration of optical components with electronic circuits. The window for pervasive deployment of converged silicon electronic-photonic technology is 2020-2025. The past 5 years has brought significant advances in co-design and process integration. A demonstrator chip using the 45nm CMOS node contained an electronic microprocessor with optical transmitter/receiver banks, couplers, photodetectors and ring modulators for memory communication. This electronic–photonic 'system-on-chip' contained 70M transistors and 850 photonic components. The 3x6mm chips were fabricated in a CMOS foundry with zero-change to the 45nm node PDK. The 45nm node is thermal budget compatible with the future introduction of Ge technology for high performance. The experiment was instructive in validating that 'good enough' photonic devices that are monolithically integrated with electronics give superior energy-delay performance relative to hybrid integration of separate subsystem chips.

CRITICAL INFRASTRUCTURE ISSUES

The maturation of silicon photonics to fully accommodate the efficiencies of the CMOS process infrastructure will be the focus of the next decade. Manufacturing system integration is the grand challenge. Standardization of materials, design packaging and functional blocks will emerge. Design at the system level with cost, energy, latency and bandwidth density as the prioritized requirements will be the new skill set.

Silicon photonics was deployed commercially in 2019 with estimated manufacturing volumes of a few million chips per year. This manufacturing is executed mostly in industrial 200 or 300 mm CMOS

foundries, with a capacity for manufacturing that is vastly larger than the current demand for silicon photonics manufacturing. This over-capacity is not a major issue since the capacity of the fabs is shared between electronic IC-production and photonic-IC production. Research institutes and research companies worldwide offer additional prototyping and small volume manufacturing services for silicon photonics on semi-industrial platforms. Critical issues are expected as demand grows for:

- silicon PICs with high level integration and/or more challenging performance requirements with variation narrow margins
- silicon PICs serving a broader range of application domains and markets

In this context four different critical issues are identified.

WORKFORCE

The technology supply chain supporting the pervasive commercial deployment of silicon photonics begins with the workforce. The worldwide silicon workforce of 350,000 technicians and engineers has little exposure to photonics, and the equally large photonics workforce is unaware of the rigid, efficient infrastructure that underlies its 50% performance/cost learning curve. There is a shortage of skilled experts in the field: manufacturing technicians, design engineers, test engineers, technology developers, PDK developers, application and system integration engineers. This issue is particularly key for companies that are relatively photonics-agnostic, such as for example a medical device company or a company developing IoT-solutions. The required workforce development infrastructure should include 1) K-12 education in photonics, 2) test and automated design software education and training community college through PhD students, 3) materials, process and packaging research opportunities at the university level and 4) industry led apprenticeship and internship opportunities for retraining and education. Today education in the field of silicon photonics is being addressed by several organizations, including AIM Academy in the US and ePIXfab in Europe. It is of critical importance to grow these activities with expansion along both skill-set and job-level dimensions.

DESIGN AUTOMATION

The Process Design Kits (PDKs) of most open-access silicon photonics foundries is still relatively limited with respect to their library of building blocks: only basic active and passive components are available and often the degree of technical validation of these components is limited. Accurate compact models are often not available. This infrastructure is in stark contrast with the world of electronic design where foundries make available extensive libraries of validated circuits to the designers of their customers. To enable first-time-right designs and to enable designs by middle level workers, there is a critical need for more sophisticated PDKs, with validated components and circuits and their compact models, covering optical, electrical and thermal behavior. Parametrized designs are also of great importance so that designs can be customized to specific needs. The Intellectual Property licensing and indemnification for the library building blocks should be transparent, so that the end-user can design in a legally secure framework. The design tools should allow for seamless compatibility with tools for electronic design or other parts of the system (packaging, RF-interaction, microfluidics, etc).

DESIGN FOR MANUFACTURABILITY AND TESTABILITY

Given the intrinsically analog nature of most photonic circuits it will become increasingly difficult to make designs that are robust against process variations, in particular for LSI photonic circuits. Ensuring a high yield of devices that satisfy the designed-for specifications will become increasingly more challenging. This critical issue needs to be addressed from two angles: the tolerances on manufacturing process steps need to go down and the design tools need to be able to perform efficient tolerance analysis and optimization for tolerance against process variations.
Testability needs to be addressed along similar lines. Generic test circuits that are added to a reticle for process monitoring may not be enough to ensure that a chip will work as foreseen. There may be a need for circuit-specific test modules that will monitor critical parameters for given circuit functions, both for in-line testing and for post-fabrication testing. As much as possible all testing should be possible at wafer level by automated probing.

EVOLUTION OF PLATFORMS

In recent research we see a very rich diversity and density of impressive achievements that boost the functionality and performance of silicon PICs for an ever growing range of applications and markets. More often than not these PICs cannot be manufactured in the existing industrial manufacturing platforms, because they require new materials or process steps that are not part of the standard process flow of these fabs. The situation is more relaxed in the research-oriented fabrication platforms. In general the MRL-level of these extended silicon photonics platforms is substantially lower than the manufacturing platforms. This situation raises the critical issue of how the manufacturing infrastructure for silicon photonics will be upgraded to address the needs of new applications and markets. There is a paradox behind this issue: silicon photonics has been successful to a considerable degree because it was possible to manufacture photonic ICs with the standard toolset of a typical CMOS fab. But very rapidly we are now facing demands for extensions that may not build on existing process knowhow and infrastructure in the CMOS-fab. Given the large non-recurrent engineering cost that an extra toolset or process development causes in a CMOS-environment, it is far from trivial to transition from research to industrial manufacturing. Therefore, it is important to develop as much as possible a platform that can be used across multiple application areas. These considerations are particularly relevant for the integration of light sources. The fact that such integration is hardly possible today in open-access foundries represents a real gap in the field. This subject is discussed further in the section on Gaps and Showstoppers.

TECHNOLOGY NEEDS

PRIORITIZED DEVELOPMENT & IMPLEMENTATION NEEDS (BEFORE OR DURING 2025)

Table 19: Prioritized Development & Implementation milestones (≤ 2025)	**Relative priority**
Design Automation Seamless compatibility must be established among digital/analog CAD tools and design rules. Lumped element device and circuit models will supplant first principles simulation to allow a wide range of designers to participate in the industry. The models should be parametric, including speed, voltage, heat, isolation and mixed signal values. Robust design should develop immunity to device/circuit/system variation. Optical impedance matching, linearity, bandwidth, noise, power, thermal management and process integration should be embedded in design rules for geometry and layout. Near term needs are: • validated PDK models for active and passive photonic circuits • models for hybrid ASIC-on-optical interposer • compatibility with evolution of SM, DP, multilevel coding, ... • foundry infrastructure: IP licensing/indemnification • look-up database; licensing fees	Critical
Multi-Project Wafer and Assembly (MPWA) The MPW process should include tightly coordinated joint development projects that explore options and implement platform solutions. • optical power supply solution • high radix matrix switch solution: > 64x64 • distributed gain block solution • I/O and power distribution for 2.5D (electronic and photonic) • SM-everywhere compatibility • athermalization, scalable tuning: filters, modulators	Critical
Inline Control and Test (ICT) Electronic and optical inspection and test must be low cost with high yield, throughput and utilization of the inspection/control system. Design for Test	Critical

• Limit test protocols using one approach for both hermetic and non-hermetic devices • Reduce test cost with rapid optical probe methods or BIST electronic probes • Reduce test with high yield Wafer level inspection • High throughput photonic test • Known good die • Reduce test capex	
Reliability and Redundancy Failure modes must be known with modeled dependencies on processing, materials and use. Fault tolerant design with low component stress levels and redundancy is essential. • Known failure modes • Early warning, fault prediction, fault tolerant design • Standard hermetic and thermal test under operation	Critical

Table 20: Prioritized Development & Implementation milestones (> 2025)	**Relative priority**
Design Automation • validated PDK models for electronic-photonic circuits • validated chip-level thermo-mechanical models • validated package-level thermo-mechanical models • single electronic-photonic IC package design platform	Critical
MPWA • Pervasive gain blocks with standard devices • I/O and Power distribution for 3D (electronic and photonic)	Critical
Wafer level inspection • Functional system qualification test • BIST: Built-in Self-Test	Critical

GAPS AND SHOWSTOPPERS

The integration of Silicon Photonic technology into the highly optimized and efficient silicon electronics supply chain and manufacturing process flow is the 'transistor of the 21st Century". Electronic-Photonic integration mates the intelligence of electronic computation and control with the high bandwidth density interconnection and broad-based sensing capabilities of photonics. Specific Gaps and Showstoppers are

listed in the Tables below (**Table 21** and **Table 22**), and related requirements are discussed further in terms of module-level, chip-level and device-level gaps. The major risk mitigation issue is establishment of a universal technology learning curve that will link scientific achievements of the future to market opportunities and build a supply chain. Two major gaps exist with two different time horizons. The first is wafer-level light source integration, with a horizon of 5-10 years after 2020. The second is the extreme driver of monolithic electronic-photonic convergence with a time horizon of 10-20 years after 2020.

Open-access manufacturing for wafer-level light source integration

Key gap: in 2020 there are no open-access industrial platforms for wafer-level integration of light sources on silicon photonics platforms. Unless this gap is resolved in the next 5-10 years a showstopper will arise for major sectors of the silicon photonics markets.

There is a very large body of research on ways to integrate light sources (mostly based on III-V semiconductors) on silicon photonics platforms. The techniques used range from the mounting of micro-optic benches (MOB) or flip-chip to bonding or transfer printing to monolithic epitaxial growth of III-V layer structures onto silicon. Some of these techniques are being used in commercial products today and have therefore reached a decent level of yield and cost-effectiveness. However, almost none of these industrial approaches is accessible for fabless companies in foundry mode, with a mature PDK and a coordinated supply chain. A 'handicap' in this context is the broad range of candidate technologies which dilutes research investment. It is very hard to predict which technologies will become dominant and within which architecture: separate optical power supply or component level integration. At one extreme one can imagine that open access supply chains will be developed for MOB- or flip chip based techniques. Their cost will probably be larger than that of the silicon PIC cost itself. At the other extreme one can envision a monolithic (epitaxy-based) approach in which the cost of the light source integration is a limited fraction of the total PIC cost. Are there may be sweet spots in between those extremes. The next 5 years will be decisive about the route towards industrial manufacturing chains for light source integration.

Electronic-photonic convergence

Key gap: in 2020 silicon photonics is not sufficiently mature for a full convergence of large-scale integration of electronic and photonic functions on a single silicon-based platform by means of monolithic integration.

Module level gaps reflect a paradox of the success of silicon. Mature solutions have been optimized and have become entrenched against change. In particular, the design, packaging and interconnect architectures is being disrupted by high capacity Silicon Photonics capabilities, and the emerging solutions are patchwork remnants from their disparate electronic and photonic originating platforms. Perhaps the most significant gap is the ramp path for 'good enough photonics' enhanced by mated electronics. A sequential list of module-level gaps to be surmounted are as follows.

- 2025: A cost reduction of 5x for packaging and interconnection
- 2025: Silicon Photonic interconnection platform: connectors and surface mount
- 2035: Internet of Things Platform: integration, power, reliability

Chip level gap solutions will be determined by the co-evolution of business models, software, hardware and architecture. For example, technology leadership for hyper-data center performance scaling at 1000x/10yr has migrated from OEMs to the large end users. However, the component R&D required for timely solutions cannot be supported by a market that has saturated at 10M units/yr. Switch bandwidth requirements double every 18 months; more bandwidth requires more lanes; short Cu links are limited to 100Gb/s; there is a *feasibility gap* for chip I/O > 50Tb/s.

Device level gaps are subject to component/system architecture solutions. The most important gap is a transparent optical I/O. Light source integration is the most disruptive challenge, and at high bandwidth density, remote, optical power supply solutions are being implemented. Thermo-optic and related sources of device performance variability are being solved by composite materials and by heater control approaches, and standard design modules are required.

- Wafer-level inspection and test
- Monolithic scaling of bandwidth density: transceiver disaggregation and DWDM
- Scalable network switches: photonic/electronic path switches; packet/circuit protocols
- THz RF functionality: low loss, high power, linear components; low RIN lasers

GAPS: MISSING CIRCUIT ELEMENTS

Table 21: Prioritized Gaps to be bridged by 2025	**Performance Target**
Gain block solution	Gain > 30dB
High radix matrix switch solution: packet + flow	Radix > 64x64
Linear, low loss, high power waveguide	Loss < 0.001dB/cm; 500mW
Design-for-Test	In-line control charts

SHOWSTOPPERS: CIRCUIT PERFORMANCE REQUIREMENTS

Table 22: Prioritized Showstoppers for 2030	**Performance Target**
Chip optical interface without fiber attach	Loss < 0.01dB
Optical power supply solution	Data rates > 1 Pb/s
Thermo-optic resiliency: filters, modulators, lasers	$\Delta\lambda$ < 1pm/K

RECOMMENDATIONS ON POTENTIAL ALTERNATIVE TECHNOLOGIES

Adoption of advanced technologies (both photonics and electronics) is primarily dependent on the integration of synergistic electronic-photonic design principles. Continued. system performance scaling through 3D integration and chip stacking compensate for the loss penalty of long (> 1mm) electronic interconnects but introduce increasing power density barriers. The operating power density for a network switch chip is ~500mW/mm^2, and an integrated optical transceiver operating at 5pJ/bit has a power density of ~100mW/mm^2. Silicon photonics currently supplants electronic interconnection where appropriate with i) distance independent cables at the system and network level, ii) high bandwidth density, board-level fly-over fiber and iii) emerging optical co-packaging for > 50Tb/s I/O.

- Optical co-packing is envisioned to enter commercial deployment in a 2.5D architecture with transceiver chiplets surrounding a central processor to minimize electrical interconnect length.
- Reliable, high density optical connectors gate the entry of optical co-packaging.
- Integration of the optical modulator and photodetector detector into the processor chip will provide further reduction in the electrical interconnect power burden.
- Monolithic integration of silicon photonics CMOS electronics provides the path to scale power, performance, area and cost.

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APPENDIX

Table A1: Overview of worldwide silicon photonics foundries and associated technologies.

(Modified from A. Rahim, T. Spuesens, R. Baets and W. Bogaerts, "Open-Access Silicon Photonics: Current Status and Emerging Initiatives," in Proceedings of the IEEE, vol. 106, no. 12, pp. 2313-2330, Dec. 2018.)

Foundry	Platform	Technology	Waveguide Layer Thickness (nm)	Wafer Size (mm)
RAPID PROTOTYPING SERVICES				
AMO	thin SOI	e-beam	220, 340	150
	SiN	e-beam	220, 300	150
Applied Nano Tools	thin SOI	e-beam	220, 300	150
CNM/VLC	SiN	I-line stepper	300	100
Cornerstone	thin SOI	248 nm	220, 340, 500	200
LIGENTEC	SiN	248 nm	up to 2500	100/150
Omega Optics	thin SOI	-	220, 230, 250	-
CMOS/MEMS PILOT LINES & RESEARCH INSTITUTES				
AIM (SUNY)	thin SOI		220	300
	SiN	-	-	300
AMF (former IME)	thin SOI	248 nm / 193 nm	220, 340	200
	SiN-on-SOI	248 nm / 193 nm	-	200
CEA-LETI	thin SOI	193 nm	310	200
	Ge/SiGe	193 nm	up to 3000	200
IHP	thin SOI	248 nm	220	200
IMEC	thin SOI	193 nm	220	200/300
	SiN	193 nm	300	200
IMECAS	thin SOI	-	220	200
INPHOTEC	thin SOI	e-beam	220	150/200
Sandia Lab	thin SOI	-	240	-
VTT	Thick SOI	UV	3000	150
INDUSTRIAL FABS				
GlobalFoundries	thin SOI	193 nm immersion /248nm	sub-100 nm	200/300
SilTerra	thin SOI	-	-	200
SMIC	thin SOI	-	340	200
TowerJazz	think SOI	193	310	300
TSMC	thin SOI	-	-	300
LioniX Int.	SiN	UV	flexible	

Table A2: Technology Option Evaluation Criteria for Heterogeneous Materials Integration of III-V-on-Si (Abdul Rahim, U Ghent/IMEC)

Techniques→	Hybrid (flip-chip) Integration				Heterogeneous integration by adhesive/direct bonding								Direct Growth of InP on Silicon			
					un-patterned III-V epitaxy (die-to-wafer bonding /transfer printing)				(semi-)processed lasers by transfer printing							
Specification	**2018**	**2020**	**2025**	**2035**	**2018**	**2020**	**2025**	**2035**	**2018**	**2020**	**2025**	**2035**	**2018**	**2020**	**2025**	**2035**
Integration process complexity																
Heat Sinking																
Integration density																
III-V material usage efficiency																
Wafer scale integration																
Laser integration process throughput																
Laser test before integration																
Option Maturity (TRL)																