ELECTRONIC-PHOTONIC DESIGN AUTOMATION

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Thanks to the many contributions and input from the various members of the workgroup and participants in the roadmapping discussion sessions.

EXECUTIVE SUMMARY

The electronic design community is large and has years of experience with ever improving commercial design tools. The photonic design community is relatively small and until recently used “homegrown” design tools or commercial tools developed for experts and researchers. To tap into the larger traditional electronic IC design community using Electronic Design Automation (EDA) solutions, the goal is to leverage well established methods and flows used in the semiconductor industry and incorporate all the relevant photonic design aspects, resulting in a unified Electronic-Photonic Design Automation (EPDA) environment.

The maturity of foundry Process Design Kits (PDKs) has improved since this roadmap was published in 2020, however their maturity is still not at the level of what is offered with contemporary Complementary Metal Oxide Semiconductor (CMOS) process nodes. Further work is required, and this mandates an orchestrated effort between foundries on one side, tasked with developing more capable and stable processes and implementing more designs, processes, and test information in PDKs, as well as software vendors on the other side, tasked with improving the tools and flows to be able to use more information from the foundries to support design for manufacturing, yield improvement, and cost reduction.

INTRODUCTION

The Electronic-Photonic Design Automation (EPDA) Technology Working Group (TWG) focuses on improving the design methodologies for scalable integrated electronic-photonic design. One of the overarching goals for improved methodologies and design tools, including Electronic Design Automation (EDA) and Photonic Design Automation (PDA) software, is to increase the number of electronic Integrated Circuit (IC) design teams in the world who integrate photonic functions into their systems, such as Application-Specific Integrated Circuits (ASICs) and System on Chips (SoCs), without requiring low-level physics design and need for employees with Ph.D. degrees in photonics. The industry is looking at foundries and software vendors to provide an environment and workflow as similar as possible to CMOS design flows.

The intention of this roadmap chapter is to identify the most critical problems and to prioritize the development of solutions to help the photonic designer community to decrease the turnaround times, improve quality of results and remove uncertainty when creating new designs for their products.

This developing designer and engineering community consists of individuals with different training backgrounds, education, and experience:

- Photonic device and process developers
- Photonic IC designers
- Electronic IC designers and engineers

Although photonic ICs are manufactured with the same type of technologies as traditional electronic ICs and a verified mask layout is also the final step of the design flow, it is important to understand the differences between designing an electrical IC and a Photonic Integrated Circuit (PIC). Given the nature of the underlying physics, a PIC is more like a millimeter wave IC operating at very high frequencies. These differences drive the need for special Photonic Design Automation (PDA) solutions in addition to existing Electronic Design Automation (EDA) solutions.

From a simplified view, the design of a (photonic) IC is a sequential multi-step approach that starts with the specification and ends with a validated and verified design in a format that can be transferred to a foundry for manufacturing. These steps are made easier for designers by means of software tools and automation steps, helping them to generate schematics and layouts, and to assess the performance of the designed chip. The term EPDA refers to an environment that supports a design team to execute a circuit design in preparation for a foundry.

Purple Brick Wall

For this chapter of the 2024 roadmap, we don’t see any fundamental Technology / Cost barrier or “Purple Brick Wall”. Most of the listed requirements are “just work” for software vendors to address. It is obvious that these vendors need to make decisions based on their customer base, ambitions and return on investment. What is not obvious however is that certain requirements can only be solved by working together as an eco-system and putting in the investment and resources to do so.

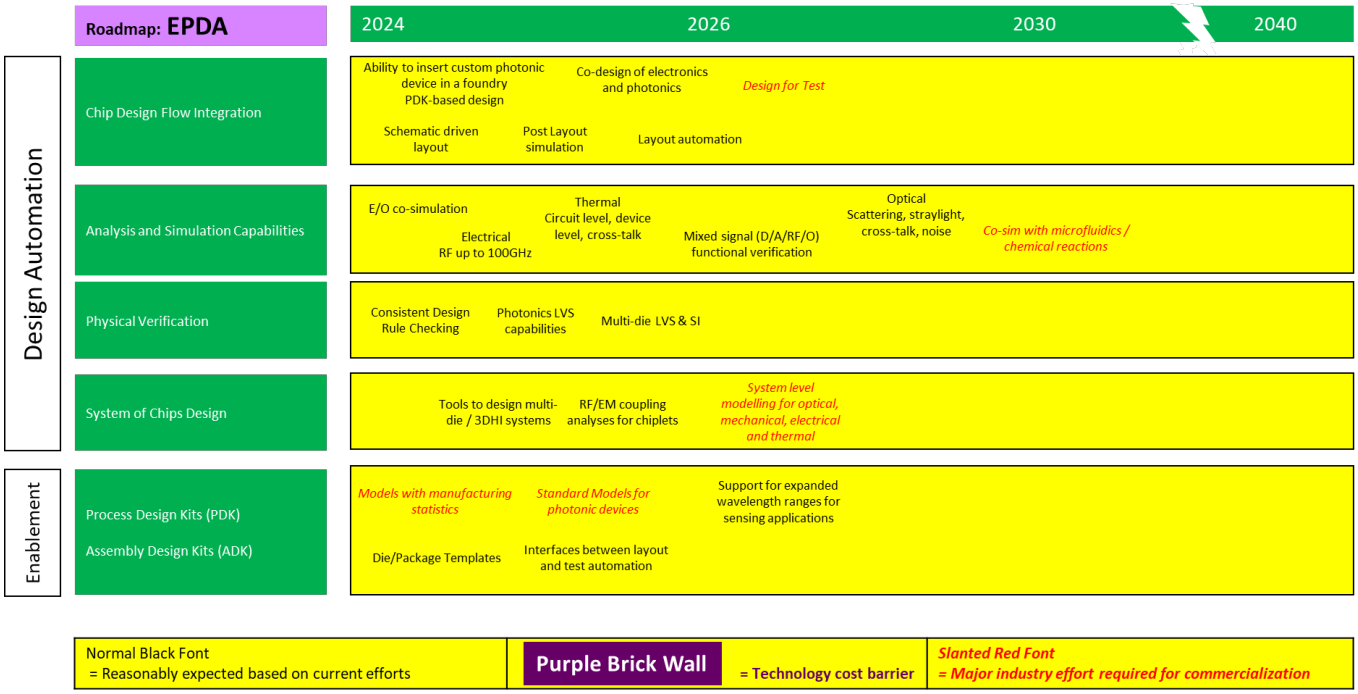

Figure 1. *Purple Brick Wall overview of Design Automation and PDK enablement items and priorities.*

SITUATIONAL (INFRASTRUCTURE) ANALYSIS

Allowing designers to create a mask layout that can be submitted to a foundry is one of the key elements for the scalability of PIC technology. The introduction of photonic Process Design Kits (PDKs) in 2008 together with Multi Project Wafer (MPW) runs has largely supported the wider application of PIC technology in domains outside the traditional telecom space and accelerated the transition from academic research into commercial manufacturing. The potential of a foundry process is largely determined by the maturity of the technology reflected in the contents of the PDK provided to its users. Such a PDK can be compatible with design software from several vendors and contains in general:

- Technology set-up files, describing the mask layers involved in the fabrication process.
- Pre-defined (Parametric and/or fixed) layouts, so called PCells or fixed Cells, respectively.
- Symbols for schematic capture and models for simulation.
- Statistical information about variations of critical parameters (tolerances).
- Manufacturing Design Rules to be able to execute manufacturing Design Rule Checking (DRC).
- Layout extraction and verification rules for Layout Versus Schematic checking (LVS).

- Parasitic extraction rules for electrical parasitics: resistance, capacitance, and inductance introduced by the metal wiring (PEX).

PIC manufacturing facilities typically offer one or more PDKs containing a component library providing the mask layout for building blocks, such as splitters, modulators, detectors, lasers, amplifiers, waveguides, etc. In the past years, more than several hundreds of designs have been fabricated based on these PDKs. This is highly successful compared to other non-traditional semiconductor technologies. In micro-electromechanical systems and microfluidics, it is still very much "one process for each application." However, to further develop the integrated photonics technology, the maturity of the PDKs needs to be improved. This requires (1) an orchestrated effort between foundries at one side, developing more capable and stable processes and adding more information on design, process, and test characteristics in PDKs, and (2) software vendors at the other side, improving the tools and flows to be able to use statistical information on process and device level, from the foundries to support design for manufacturing, yield, and cost.

A PDK supports re-use of knowledge and promotes tool interoperability, while ensuring building block performance and thus circuit yield. Foundry PDKs can also be extended by adding the design libraries from external design houses and IP providers or the design team.

Unique Characteristics of Photonics Design

As highlighted previously, the physics of photonics differs significantly from that of electronics. Recall that the telecom C-Band used in optical fiber communication centers around a 1550nm wavelength, corresponding to a frequency of approximately 193THz. This requires different time steps than electronics when simulating circuits. Optical signals can be bi-directional and multi-modal, requiring other simulation techniques and solvers. Photons are lost at sharp waveguide bends, so geometries tend to be curvilinear and the layout together with physical verification tools need to be able to cope with this peculiarity. Therefore, several dedicated solutions have been developed since the early 1990s to replace home-grown tools used in academia and research departments.

Depending on the scope of the design task, it is important to be able to switch between levels of abstraction and various PIC design aspects, such as circuit layout, circuit simulation, individual devices performance, thermal behavior study, electronic-photonic interaction, etc. To meet these needs, software tools for different design tasks must ideally integrate into and end-to-end design workflow. Essential components for interoperability are standard design databases and model libraries and adequate application programming interfaces (APIs) that enable automated interfacing between various software solutions.

Component Simulation

Device or component simulations to support PDK creation and to allow designers to add their own building blocks while designing a PIC are well-developed. For passive devices that are restricted to photonic performance, there is a wide range of commercial tools that provide accurate physical simulation results. Various numerical methods can be tailored to the specific problems. Tools do now exist to model most of the complex physical process involved in the static and dynamic operation of an active components. However, there is still a lack of measurement data from fabs that could be used to calibrate the sophisticated models involved. Without this calibration, these more complex models remain inaccessible to the less experienced PIC designer. As a result, proper simulation requires more in-depth knowledge about the device operation, to judge which approximations are justified.

Circuit Simulation

Models to simulate building blocks at the circuit level for both frequency and time domains are becoming more available, thus enabling a full design flow from circuit design to layout verification. To further develop the automation of PIC design, tools and flows activities are ongoing at several software vendors, design houses and academia, supporting PDK-driven layouts as well as custom designs within the boundaries of the fabrication technology. Depending on the end application and complexity of the system-under-design (e.g. the number of components, the required optical and electrical routing, or the balance between the components of both types), the most applicable tools or flows might be different. Electro – optical co-simulation at the circuit level has become more important, given commercial offerings of monolithic silicon photonics and the desire to co-optimize the performance of the driver and read-out electronics with the photonics.

Design Implementation

The increasing complexity of PIC designs over the last few years has resulted in design flows to move from layout-only or layout-first to a Schematic Driven Layout (SDL) flow. This is the most widely used methodology in analog chip design and starts with capturing a schematic or symbolic view of the design, that can be used to run circuit simulations and will act as the golden reference for the whole design cycle. From this schematic, the layout can be created, and software tools enforce that schematic and layout are always in sync. This allows for post-layout simulation, to validate circuit level performance after having finished the layout implementation. Such an SDL flow also allows for separation of concerns and teams with different skills (design, layout, simulation) to work closely together.

Physical Verification

Design validation with DRC and LVS needs to be implemented. In the early days of EPDA, there were challenges with DRC for the curvilinear designs that are so widespread in photonics. Today this is considered a solved problem when the foundry codes the design rules appropriately for the supported software tools. Photonic LVS is emerging, and foundries are starting to establish methods and add rules in their physical verification decks. These LVS rules and methods are not as sophisticated as those found in electronics, and additional work across software vendors and foundries will be required to further mature the rules and their implementations.

System & Functional Verification

Evaluating a designed PIC as part of a complete system is equally important. When, for example, designing PICs to be used as optical transceiver for a fiber-based communication link. System verification may include optimizing the system performance by adjusting PIC parameters and studying the system's robustness to PIC fabrication imperfections. Such simulations require an extended library of simulation models (for example, models for single- and multimode fibers, free-space optical channels), means of state-of-the-art data stream coding, modulation, detection techniques, and characterization techniques, like for example Transmitter and Dispersion Eye Closure Quaternary (TDECQ), to assess the system metrics in compliance with industry standards. In case a designer is looking to evaluate the performance of a PIC in the context of a system of chips, including the analog and digital circuitry to control, drive and read-out the optical signals and photonic behavior, functional verification solutions are used to analyze the overall behavior including the electrical domain.

ROADMAP OF KEY ATTRIBUTES AND TECHNOLOGY NEEDS

To target a larger set of designers, also from the existing IC design community, the goal for EPDA should be to rely mainly on abstracted simulation models and libraries with provided components as PCells. Detailed modeling of photonic structures plays a more important role in comparison to its electrical analog counterpart at this point. As the photonics industry matures, this level of modeling will be mostly relegated to the research and development teams and organizations rather than the design groups. The same will likely be true for (new and custom) device development as described below.

Given the nature of photonics, with a strong relationship between performance and geometrical properties, PDKs from foundries often do not have all the required devices defined. Therefore, it is often the case that custom components need to be created. This requires detailed device level modeling, which takes a considerable time to create abstracted or compact models to be combined with a model library from a foundry. Given this situation, a comprehensive EPDA solution should allow for custom device design as part of the overall solution. Either in an integrated manner, like often seen in for example inductor design for RFIC design, or to accommodate detailed modeling of components outside of the environment and allow designers to bring in their own device layouts and models. The industry needs to realize, at this point in its evolution, that these functions are necessary and that much more device modeling will be required until this technology has reached a higher maturity level.

Near Term Roadmap Priorities

To address the increasing complexity of photonic circuits, design tools will have to be able to automate more designer tasks at the circuit level. Schematic driven layout has already been mentioned as a first step and it is foreseen that additional capabilities for circuit simulation, like thermal and mechanical modeling capabilities for circuit level simulations is required to design more robust circuits for a wider operating range.

Maturity of device models used in circuit simulation is an important enabler for a schematic driven design flow based on a predefined PDK library. Today, the users of a PDK have limited visibility on how well the model reflects the fabricated device. Therefore, it is important to set steps towards a higher model quality, where a designer has visibility on what ‘level’ of models is available in a PDK (e.g., basic analytical, more elaborate physical, physical with parasitic effects included, etc.). Additionally, information on what extent of data was used to build the model (e.g., simulation only, limited # dies tested, tested over 1000s of wafers, etc.) is critical to guide chip designers.

In addition to the improvements in the circuit design and simulation environment, more automation is required for the layout phase. As circuit complexity increases, more placement of components is needed, and more interconnections need to be made. A photonic equivalent of Place and Route or even Synthesis is a feature that starts to gain more appeal in the industry. We expect to see more automatic layout generation from schematics, more auto-routing of waveguides and the electrical connections.

For most integrated end-to-end design flows and extended PDKs, collaboration is a key enabler. The PDAFlow Foundation (www.pdaflow.org), created in 2013 and including many software vendors in the field as members, started to develop and maintain standards and interfaces for defining photonic PDK exchange formats (like xPDK) that are compatible with software tools from multiple vendors. More recent initiatives at IEEE and by opened (www.openepda.org) are illustrating the transitioning in this field and the tendency to work together to improve the design environment. Besides these achievements, bilateral collaborations between software vendors exist to develop electronic-photonic design environments and/or interface layout and simulation tools. Further automation of the design flow will require more enhanced simulation routines combining time domain, frequency domain, co-simulation of electronic and photonic components, and consideration of parasitic effects, such as crosstalk and scattering. However, the priority needs to be on adding simulation capabilities to analyze performance variations because of manufacturing and operating variations throughout the whole design flow.

This requires foundries to add this information into their PDKs and the software tools to be able to use this information to perform full yield analysis.

Based on the IPSR-I working group meetings the priorities shown in Table 1 and 2 below have been identified.

***Table 1**: Development milestones and respective level of priority*.

Prioritized development milestones (<2026)	Relative Priority
1. Interfaces / integration between electronics and photonic design tools	
a. Enable non-expert designers	Regular
b. Allow co-design of electronics and photonics	Critical
c. Enable E/O co-simulation and co-optimization	Critical
2. Improved verification capabilities	
a. Post Layout Simulation	Critical
b. Layout versus Schematic (LVS)	Critical
3. Automated interfaces between device and circuit simulation tools, to allow custom device design	Regular
4. Ability to extract and/or deal with 'parasitics'	
a. Optical: reflections, scattering, straylight, cross-talk, noise	Desirable
b. Electrical: RF up to 100GHz	Regular
c. Thermal and mechanical: Circuit level analysis	Critical

***Table 2**: Directions for solutions to be implemented in the short term.*

Short Term Solution Directions for identified Critical Needs

• Introduce Schematic Driven Layout
• Improve PDKs
  ○ Support for wavelengths beyond tele-/datacom to support application in sensing, quantum and RF photonics
  ○ Quality of models (process variations, multi-wavelength, thermal)
• Back annotation of actual layout implementation for post layout simulation
• Automate Layout (Place & Route, Synthesis)
• Address photonic LVS
  ○ Recognition of unique characteristics of photonics (vs. electronics), such as the potential for crosstalk between proximal waveguides
  ○ Photonic device recognition and parameter extraction

Longer Term Roadmap Priorities

The need for design, test and packaging continues to gain prominence. This includes, for instance, the ability to simulate Radio Frequency (RF) signals to and from the chip throughout the package to a printed circuit board or an electrical die in the same package. Additionally, optical (ray tracing), mechanical, electrical (charge mobility) and thermal modeling of a complete sub-systems or systems are required to develop more complex systems implementing PICs.

Beyond the support to design a "PIC in a package" the industry is trending towards building multi-die systems using Three-Dimensional Heterogeneous Integration (3DHI), resulting in "Systems of Chips." Assembling chips/chiplets with digital, analog, RF and photonic functions manufactured in different material systems (silicon, III-V's and other) creates a whole other layer of design complexity that the industry will need to address with tools, enablement, and reference flows.

There are several subjects which are of essential importance and can be qualified as the critical challenges for the next 3 – 8 years.

1. Design flows and tools must be developed for all levels and interchangeable between the several photonic technologies like Indium Phosphide (InP), Silicon Nitride (SiN), Silicon Photonics (SiPho), Thin Film Lithium Niobate (TFLN), Gallium Arsenide (GaAs), Planar Lightwave Circuit (PLC) and Polymers.
2. The merge of semiconductor electronics with photonics becomes of extreme importance. All photonic technologies and the tooling must be useable for photonic-electronic co-design.
3. The intermediate coherence between all the device aspects, like thermal management, performance of the PICs and ICs, packaging and co-designs of electronics, becomes very important.
4. The predictability and reproducibility of what a designer creates for a given manufacturing process must be improved for all technologies and levels to be able to deliver to mass markets with the mature expectations for product quality and reliability. This requires close collaboration between designers, software vendors and most importantly the foundries.

5. And finally, but not last, enough educated designers that are able to design PICs and PIC-based systems using the developed EPDA solutions.

***Table 3**: Directions for solutions to be implemented in the long term.*

Technology Development Needs (~2030)
Scale the design environment to support system design • Software tools to address the design of die/chiplet/interposer configurations • Software tools to address packaging and assembly of modules • PDKs or Assembly Design Kits (ADK) to be completed with 'models' capturing electrical, mechanical, optical, thermal phenomena and performance • Tools should allow for broadly understood design for product accounting for Design for Test, Design for Package, Design for Manufacture (DfX)