PSMC

Photonic Systems Manufacturing Consortium

Assembly & Test TWG Webinar

Richard Otte
Promex Industries Inc.
PSMC Roadmap Presentation
November 17, 2015

Driving Photonics Manufacturing

Assembly & Test of Optical Products Focusing on Minimizing Cost

Minimizing Product Cost

- Minimize the number of parts to purchase and assemble.
  - The cost of the parts, not assembly, dominates the total cost of many photonic products.
  - The higher the levels of integration for a product, the lower the individual part cost.
- But
  - Integration requires high volume to recover the up-front investment in technology, design, equipment and process development.

Reducing Assembly Costs

- Reduce the Number of Parts To Assemble:
  - Integrate !!
  - Eliminate Pigtails !!
  - Unfortunately we do not yet know how to build all of the functionality required using integration.
- So
  - **Heterogeneous Integration Is Needed and That Means Assembly.**
- But
  - Continue minimizing the number of parts

Optical vs Electronic Needs

Electronic equipment, processes, materials are well developed, so let's use electronic Assembly methods.

However,

Optical products Differ from Electronic products

- **Many optical assemblies require sub micron assembly accuracy and mechanical stability, especially those utilizing SM technology.**
- **The Z dimensions is often used.**

But

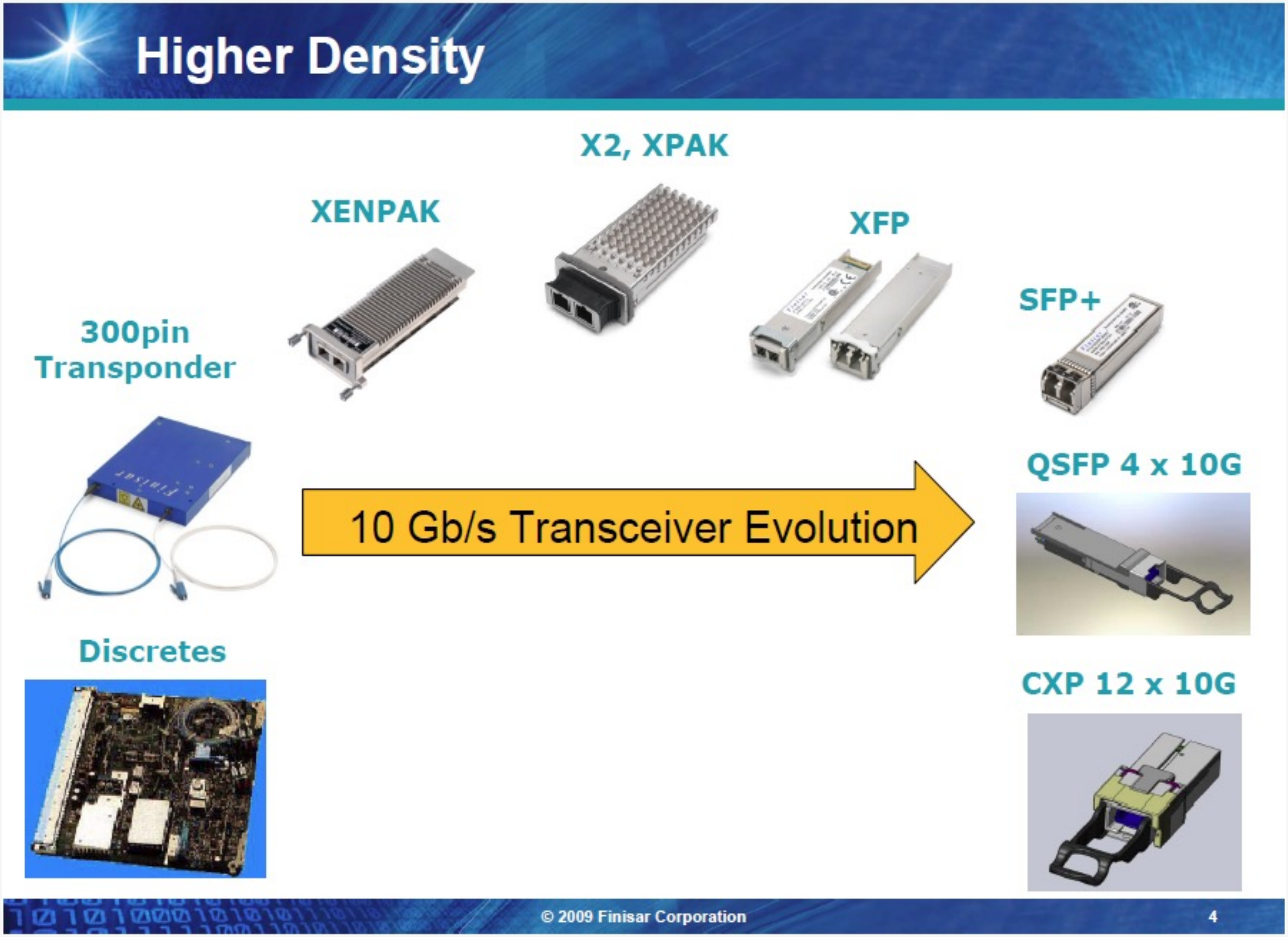
- **As long a electrical conductors maintain continuity, they can flex with temperature and mechanical stress.**
- **Historically, electronic devices have been designed to flex under these stresses.**

So

- **the Presentation concentrates on the issues, needs and methods to achieve the sub micron stability frequently required in optical products.**

What We Build Now

Transceivers !



Higher Density

Discretes

300pin Transponder

XENPAK

X2, XPAK

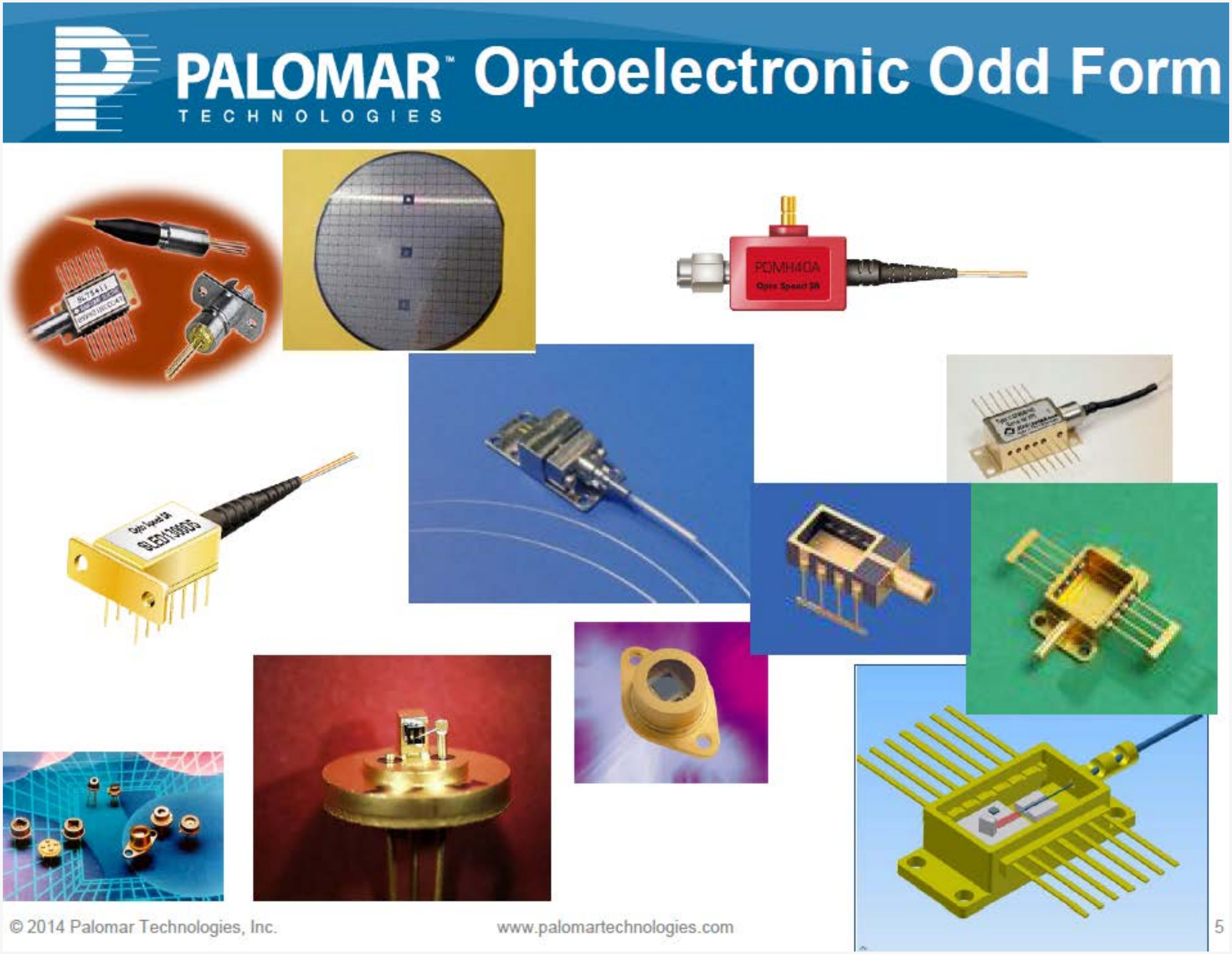
XFP

SFP+

QSFP 4 x 10G

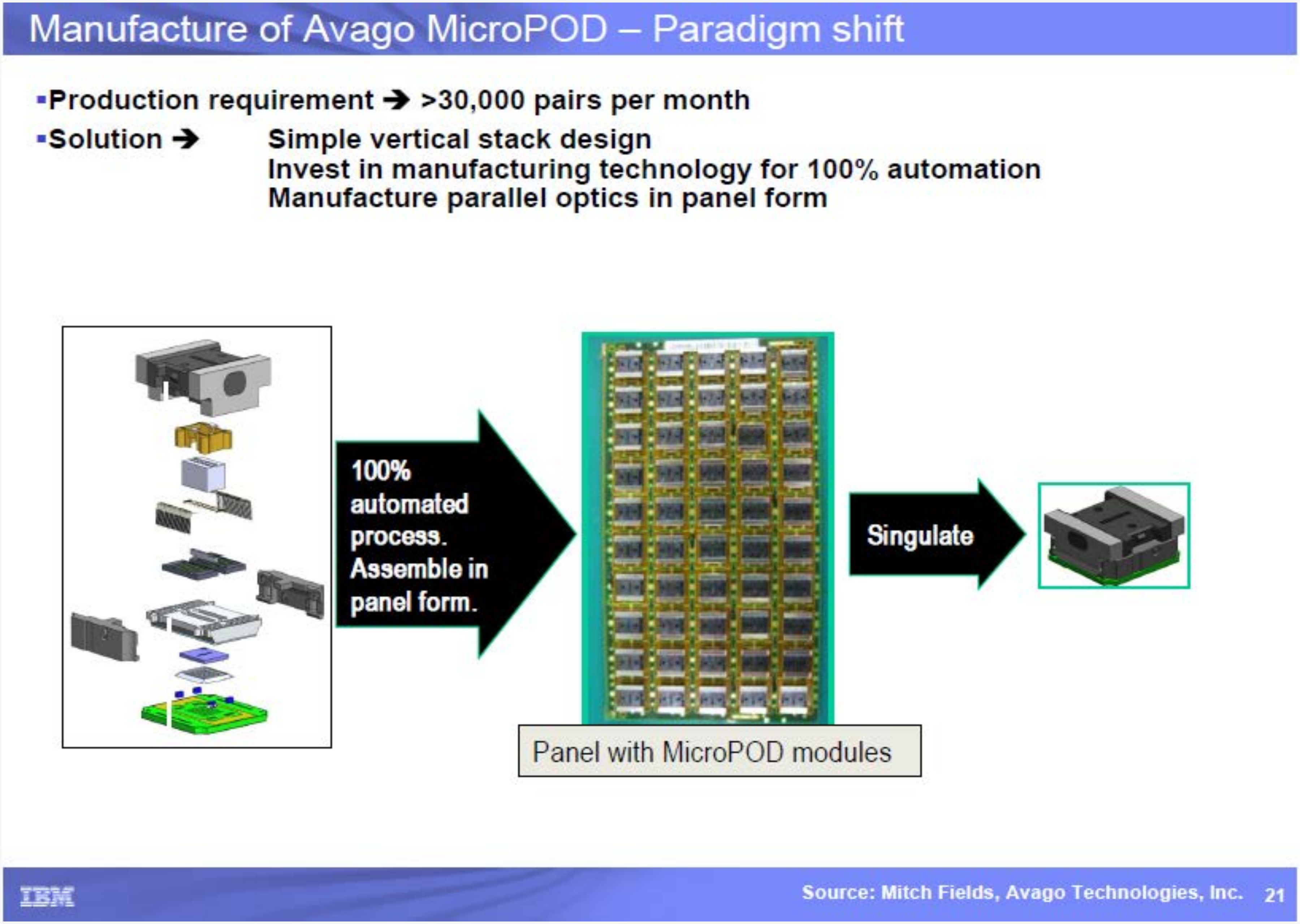
CXP 12 x 10G

10 Gb/s Transceiver Evolution



PALOMAR TECHNOLOGIES Optoelectronic Odd Form

www.palomartechnologies.com



Manufacture of Avago MicroPOD – Paradigm shift

- **Production requirement ➔ >30,000 pairs per month**
- **Solution ➔**
  - **Simple vertical stack design**
  - **Invest in manufacturing technology for 100% automation**
  - **Manufacture parallel optics in panel form**

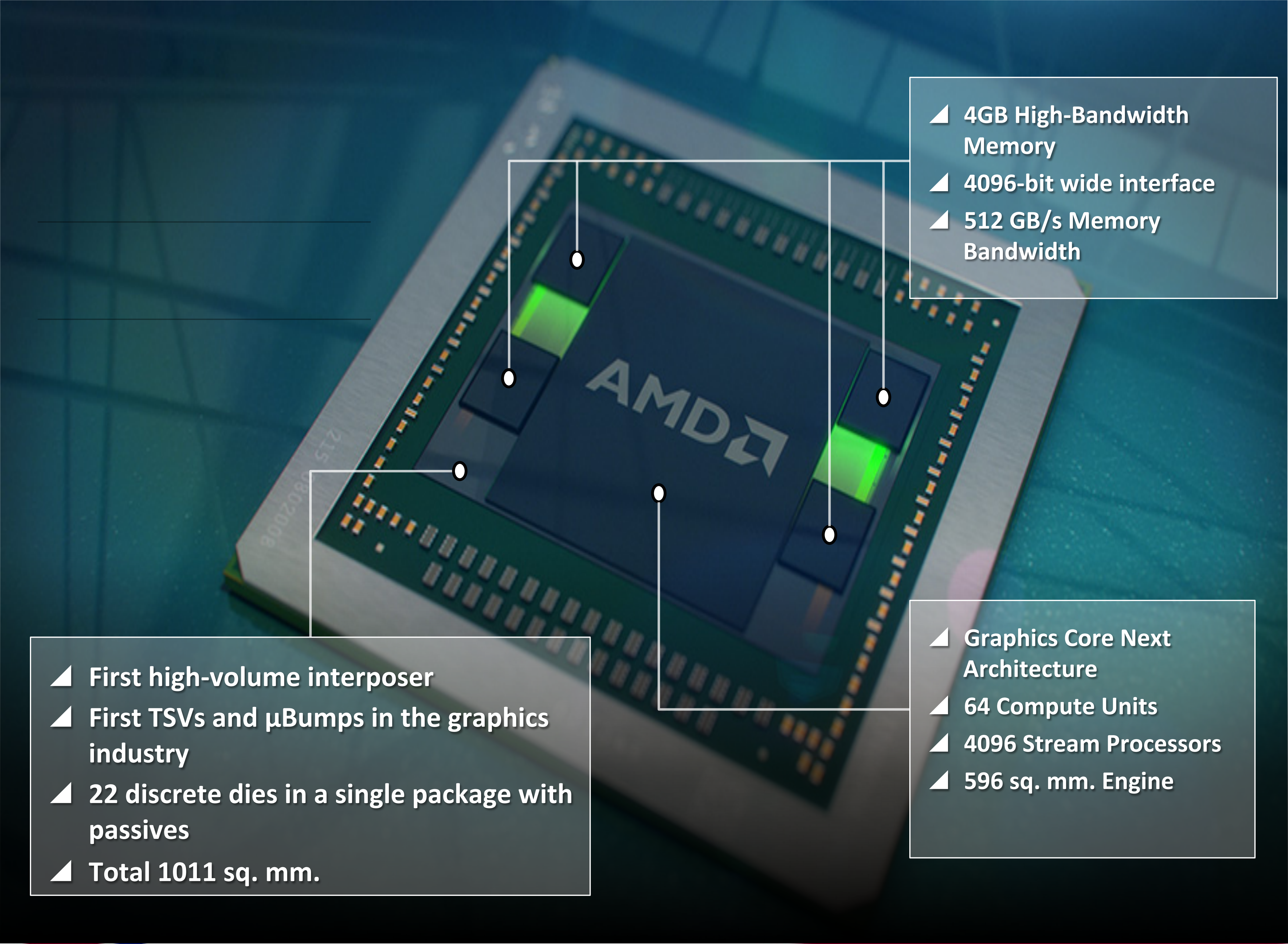
100% automated process. Assemble in panel form.

Singulate

Panel with MicroPOD modules

IBM

Source: Mitch Fields, Avago Technologies, Inc.



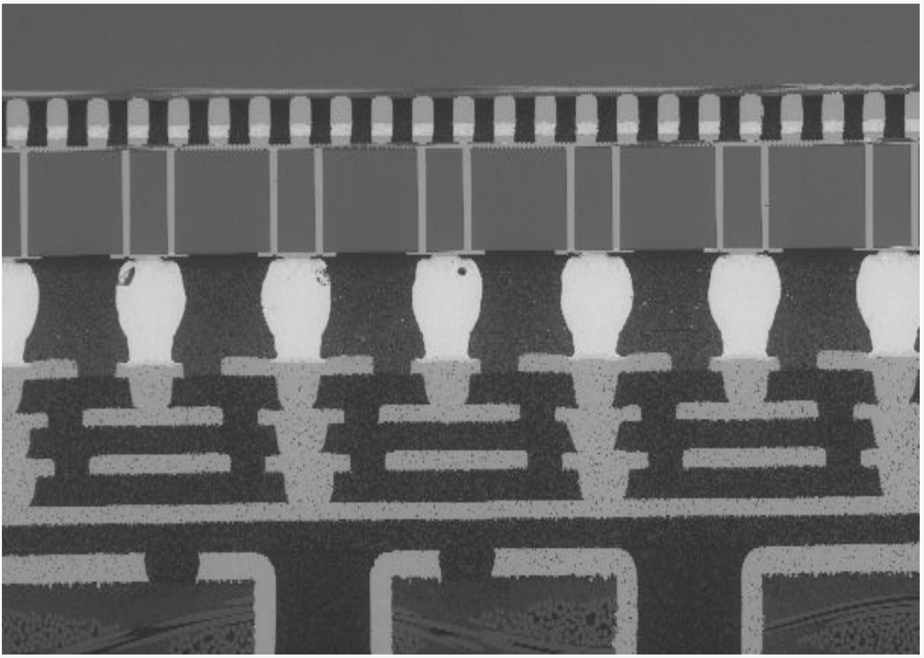
- 4GB High-Bandwidth Memory
- 4096-bit wide interface
- 512 GB/s Memory Bandwidth

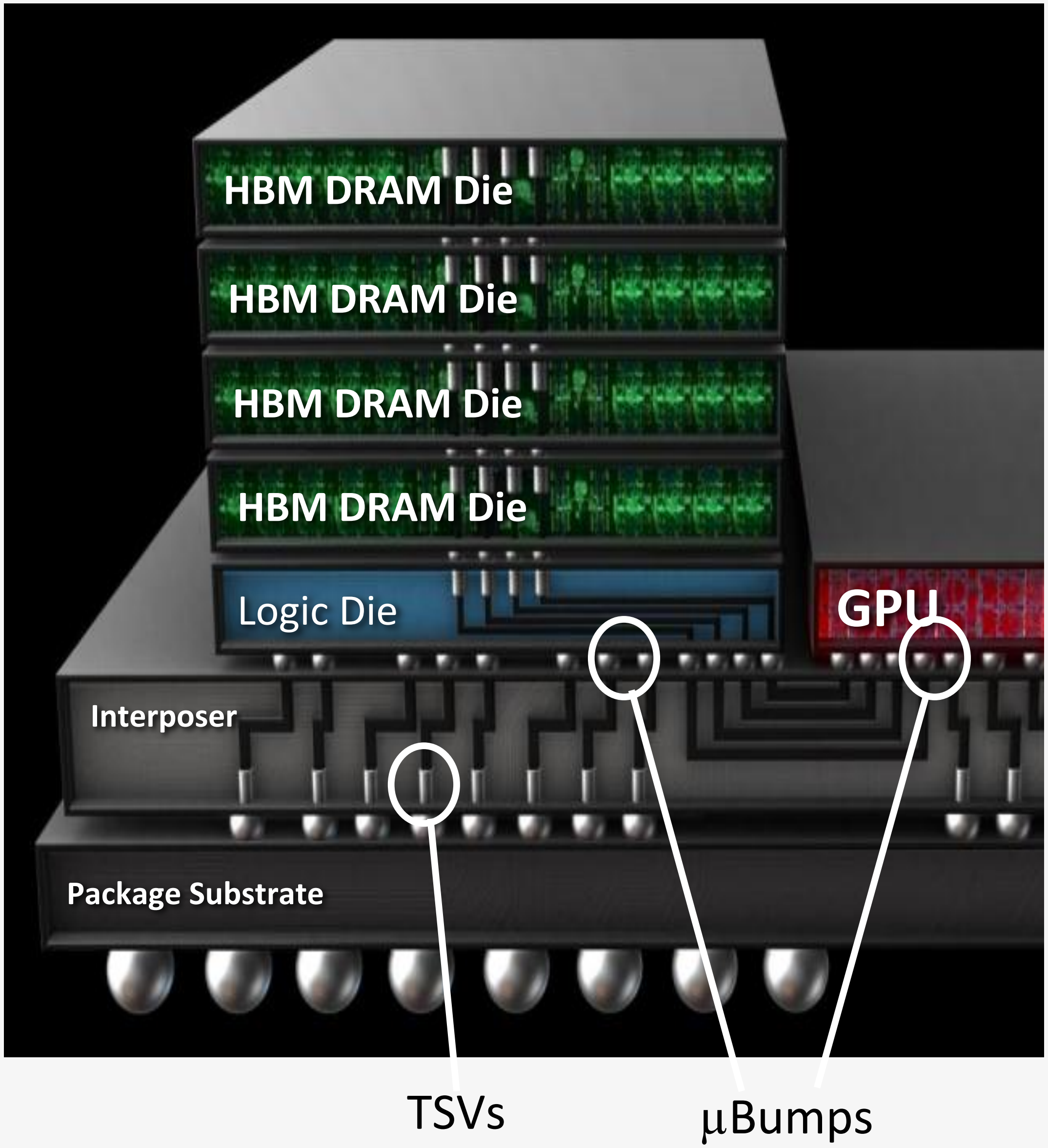
- First high-volume interposer
- First TSVs and µBumps in the graphics industry
- 22 discrete dies in a single package with passives
- Total 1011 sq. mm.

- Graphics Core Next Architecture
- 64 Compute Units
- 4096 Stream Processors
- 596 sq. mm. Engine

3D Die Stacking Technology (AMD FiJI)

- ✓ Die stacking facilitating the integration of discrete dies and passives
- ✓ 8.5 years of development by AMD and its technology partners

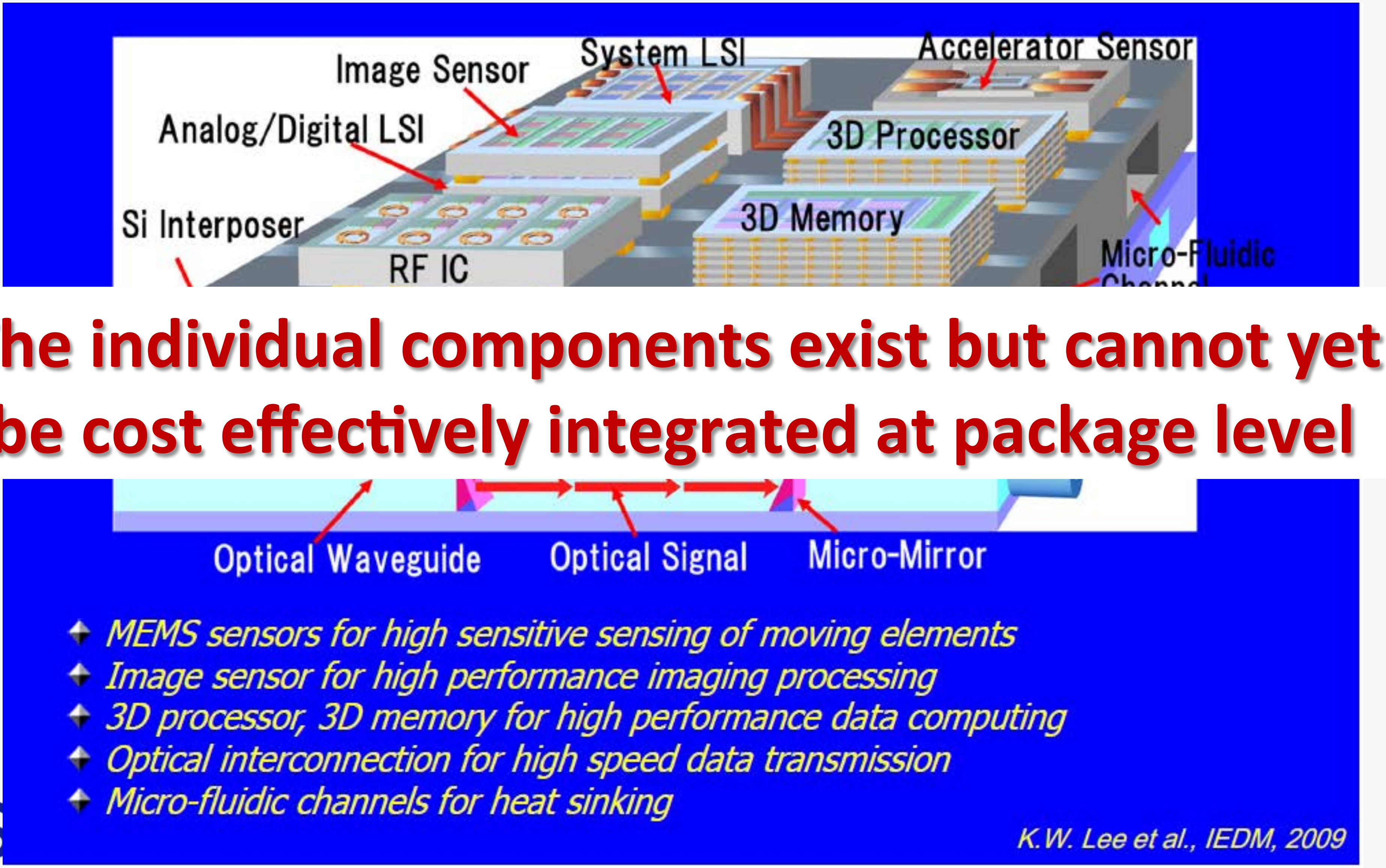




What We May/Will Build

3D-SiP Heterogeneous Integration Concept

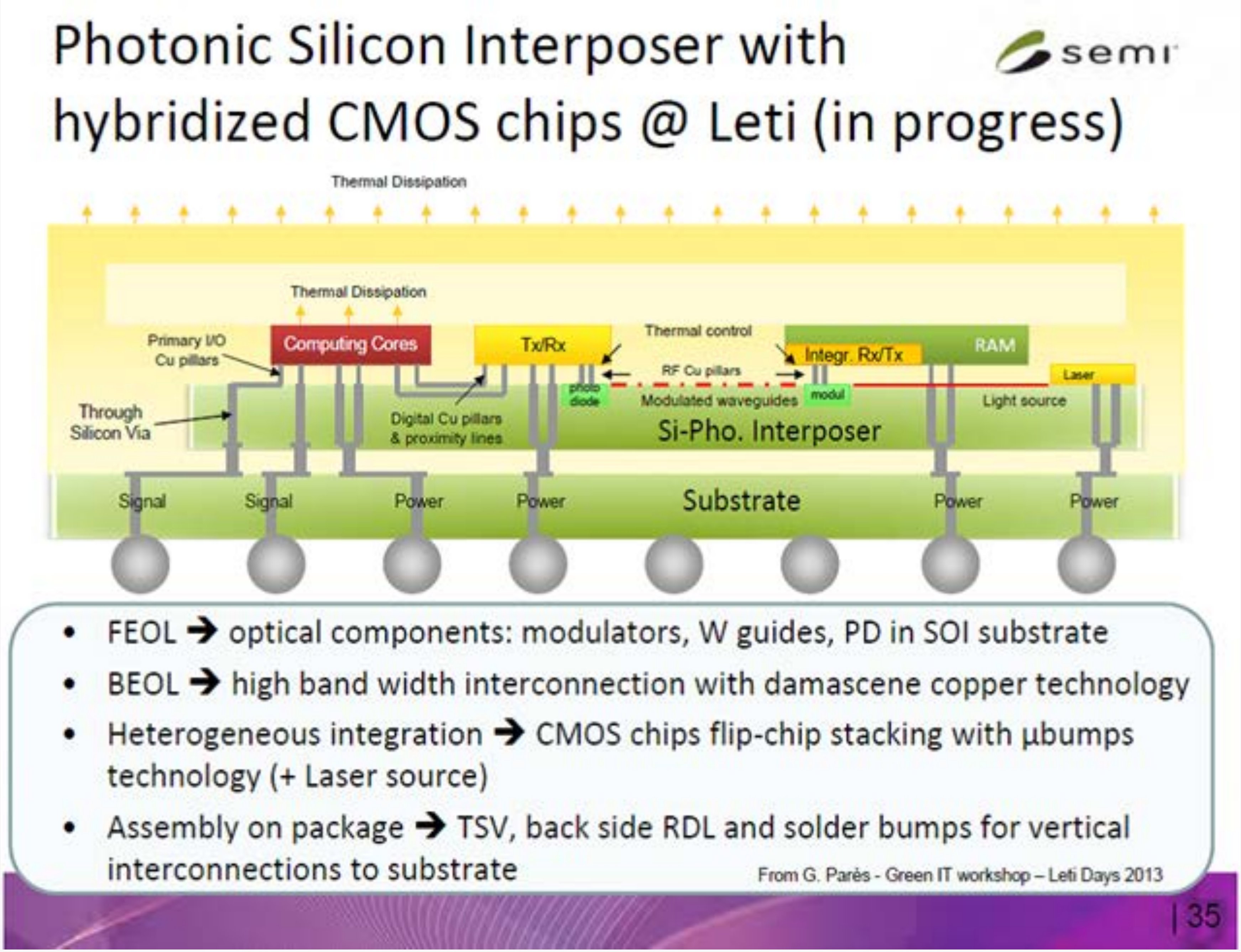
This may be the HI package of the future



- *MEMS sensors for high sensitive sensing of moving elements*
- *Image sensor for high performance imaging processing*
- *3D processor, 3D memory for high performance data computing*
- *Optical interconnection for high speed data transmission*
- *Micro-fluidic channels for heat sinking*

K.W. Lee et al., IEDM, 2009

The individual components exist but cannot yet be cost effectively integrated at package level



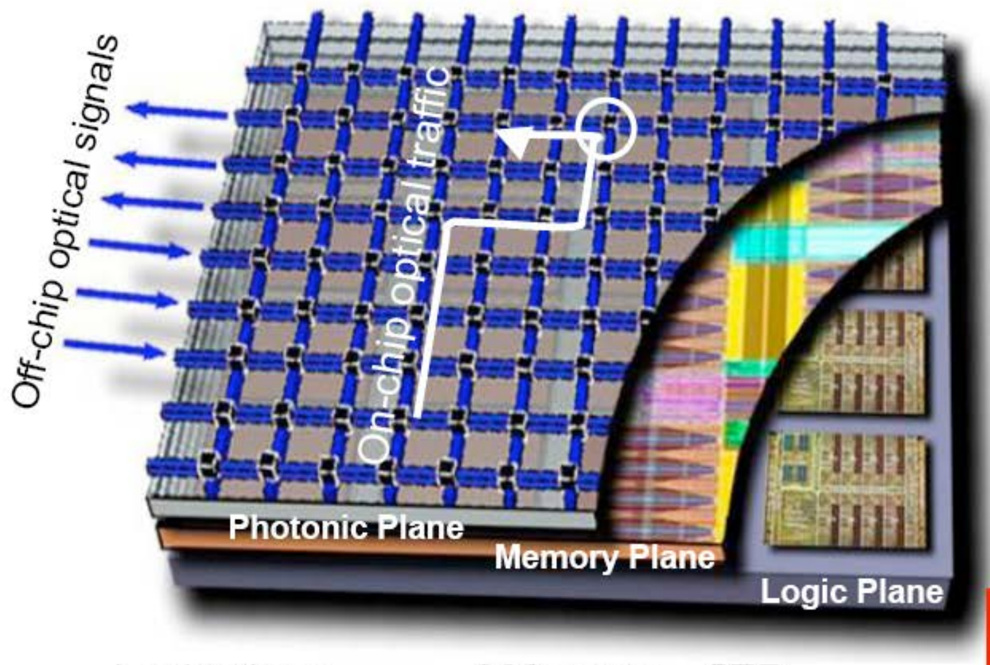
Photonic Silicon Interposer with hybridized CMOS chips @ Leti (in progress)

- FEOL → optical components: modulators, W guides, PD in SOI substrate
- BEOL → high band width interconnection with damascene copper technology
- Heterogeneous integration → CMOS chips flip-chip stacking with µbumps technology (+ Laser source)
- Assembly on package → TSV, back side RDL and solder bumps for vertical interconnections to substrate

From G. Parès - Green IT workshop – Leti Days 2013

Vision for 2020 – Optically connected 3-D Supercomputer Chip

2020	**1mW/Gb/s**	**$0.025/Gb/s**



- **36 “Cell” 3-D chip**
- **Silicon photonics layer integrated with high performance logic and memory layers**
- **Layers separately optimized for performance and yield**

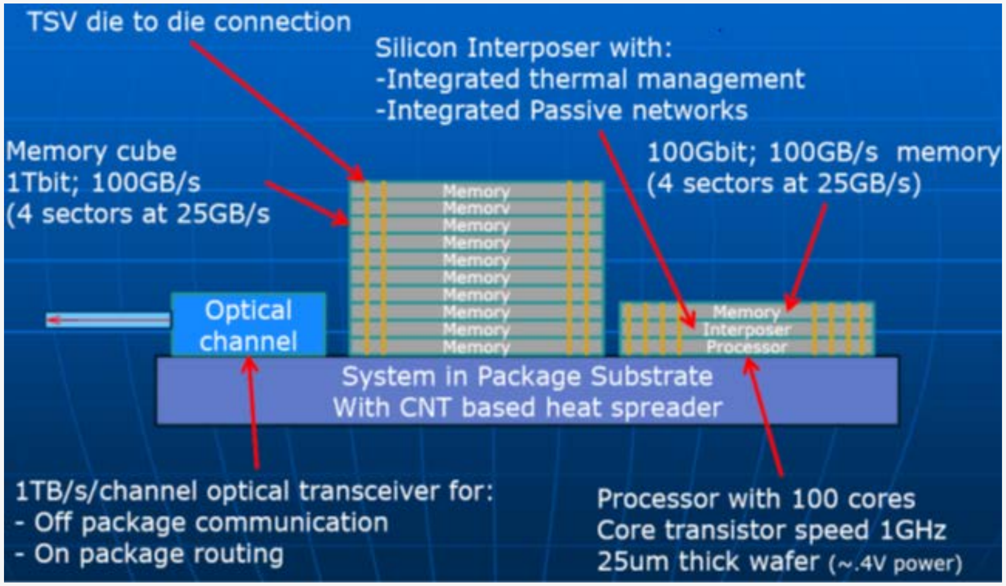
Photonic layer not only connects the multiple cores, but also routes the traffic

Logic plane	~300 cores, ~5TF (36 “supercores”)
Memory plane	~30GB eDRAM
Photonic plane	On-Chip Optical Network >20 Tbps (bidirectional) optical on-chip (between supercores) >20 Tbps optical off-chip

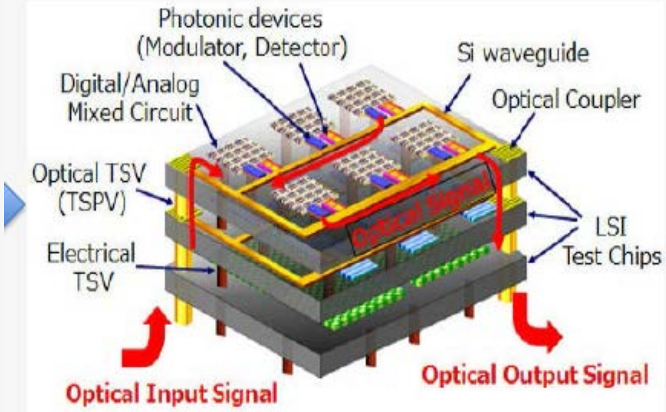
System level study:
IBM, Columbia, Cornell, UCSB

Potential Structures to Assemble & Test

Figure 4. Conventional BGA Packaged Device Mounted on an Optical Interposer to Enable Optical IO to Interface to a Circuit Board Containing Waveguides.

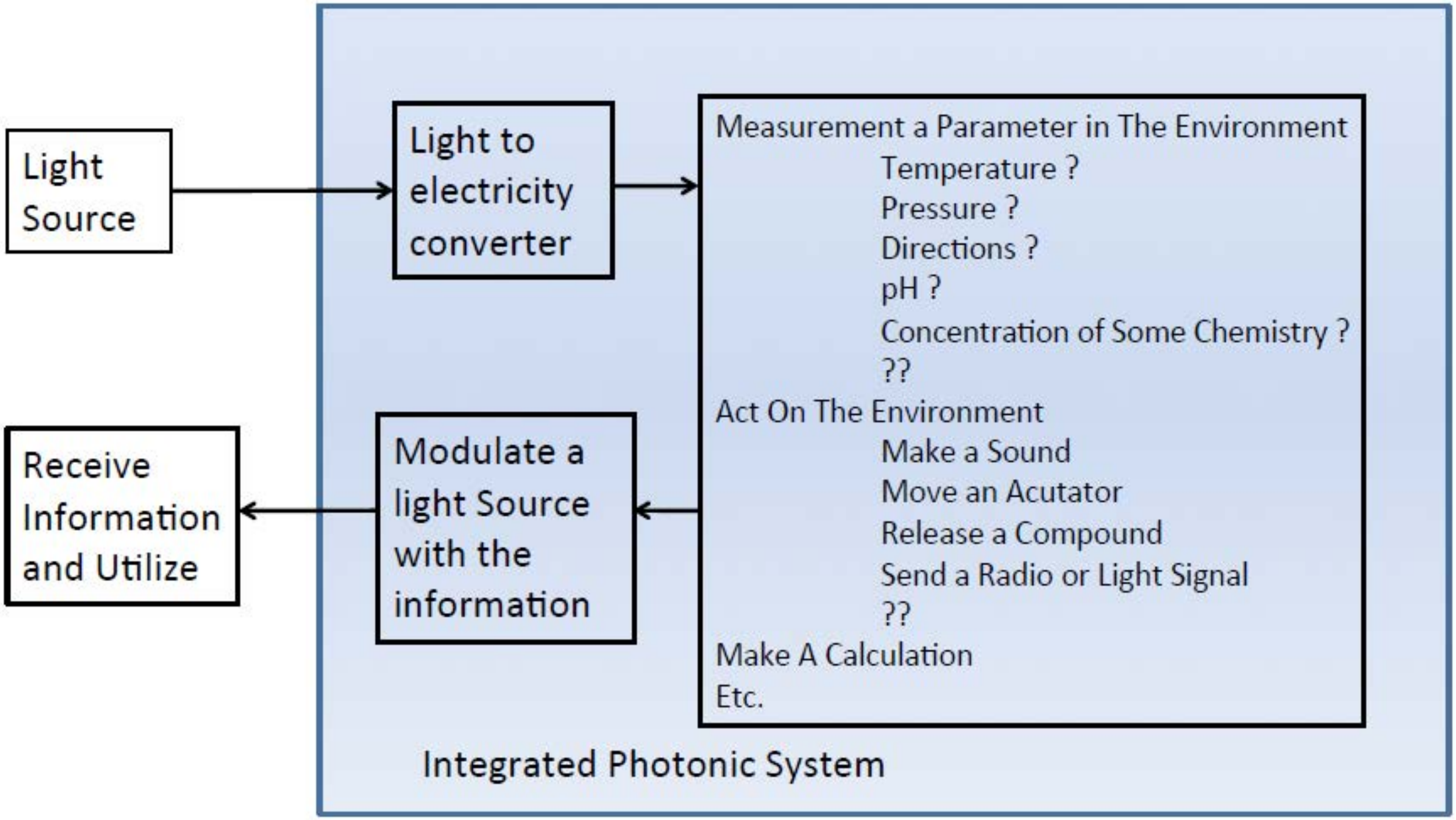


Future



Optical engines on an electro-optical package substrate interconnected with system level components

Build IPS that can be Powered by Light, Sense a Property, Send Information Back



Light Source

Light to electricity converter

Measurement a Parameter in The Environment
- Temperature ?
- Pressure ?
- Directions ?
- pH ?
- Concentration of Some Chemistry ?
- ??

Act On The Environment
- Make a Sound
- Move an Acutator
- Release a Compound
- Send a Radio or Light Signal
- ??

Make A Calculation

Etc.

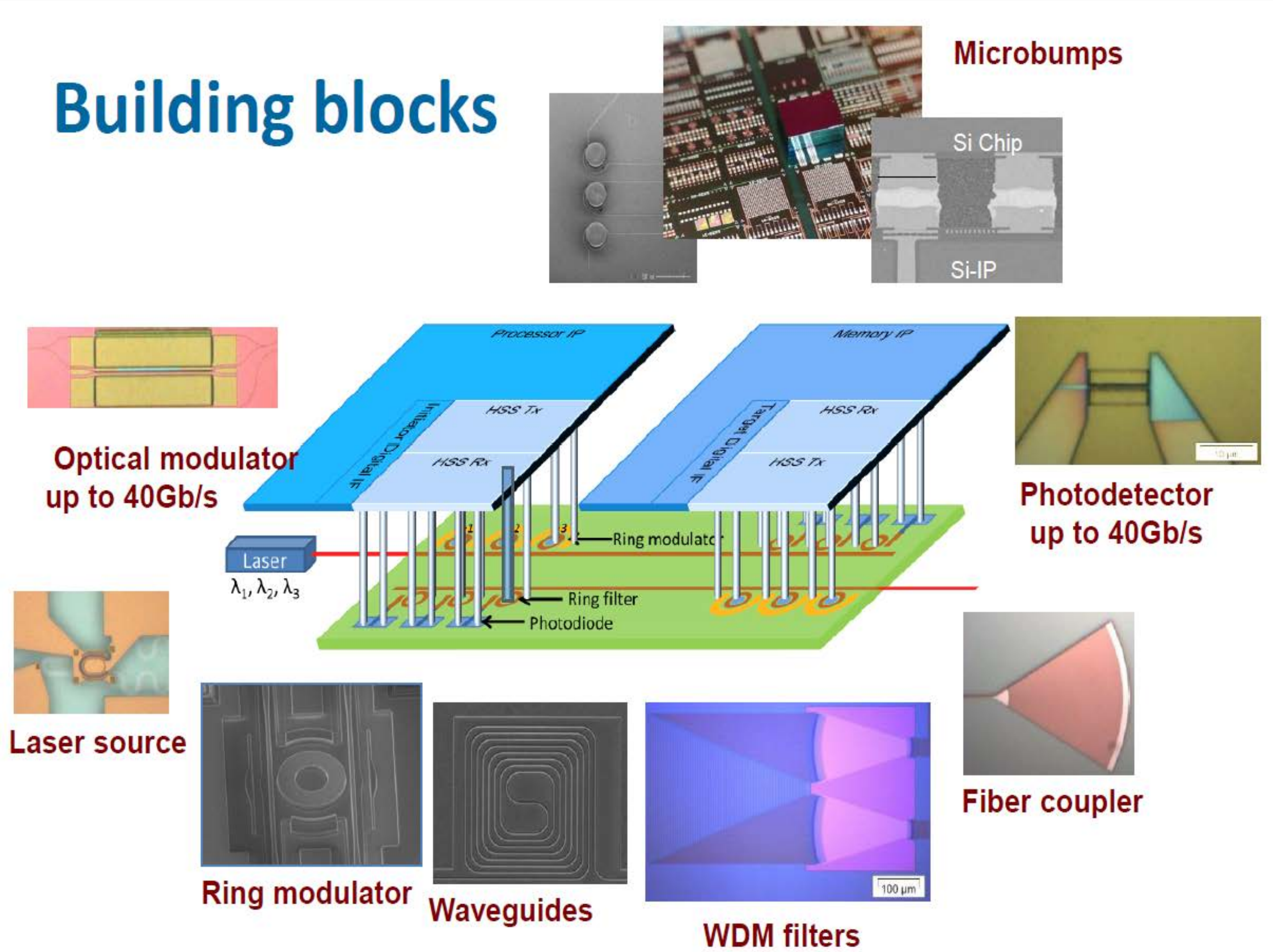
Modulate a light Source with the information

Receive Information and Utilize

Integrated Photonic System

The Parts We May/Will Need to Assemble & Test

The Building Blocks For Integrating Photonics into SiP



Building blocks

Microbumps

Optical modulator up to 40Gb/s

Photodetector up to 40Gb/s

Laser source

Fiber coupler

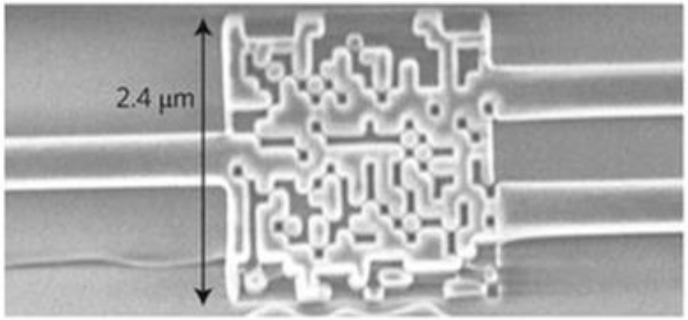
Ring modulator

Waveguides

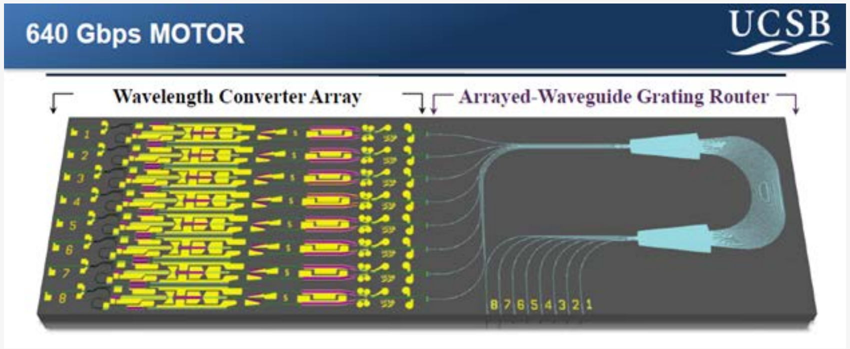
WDM filters

Source: ECTC2014 - Stephane BERNABE

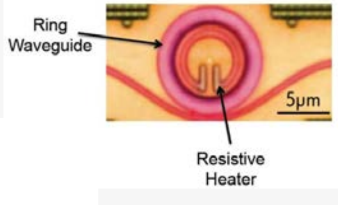
The Building Blocks For Integrating Photonics into SiP



Beam splitters



Active Wavelength Locking



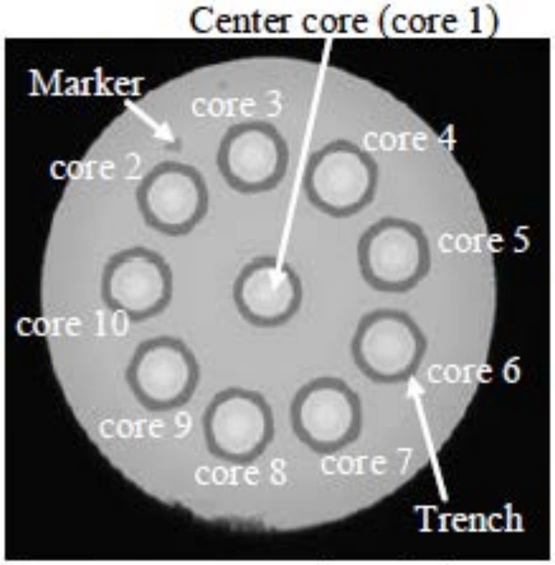
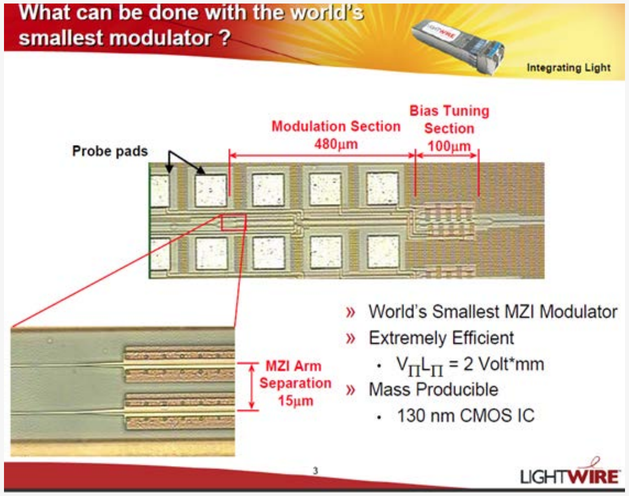


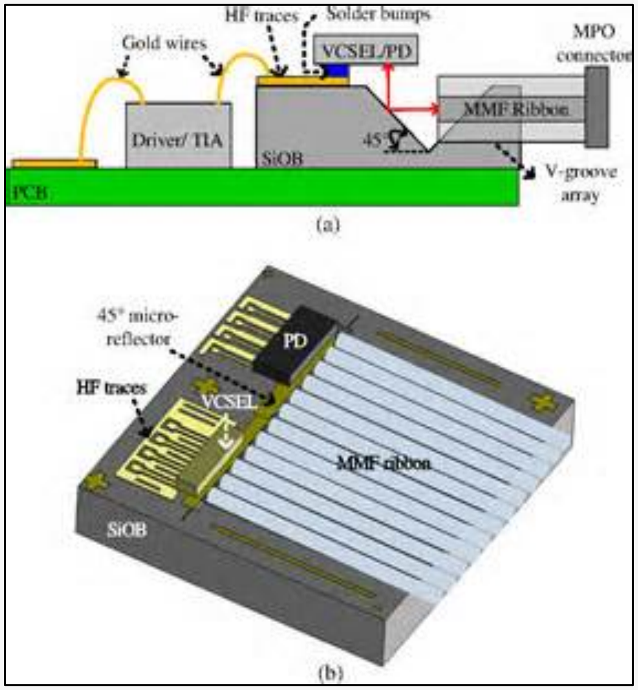
Fig.5 A cross-sectional view of a fabricated fiber.

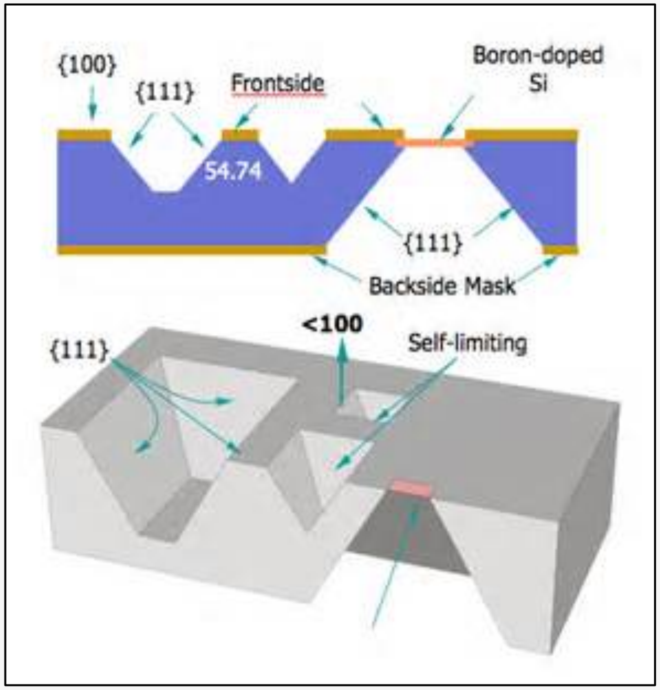

What can be done with the world's smallest modulator ?

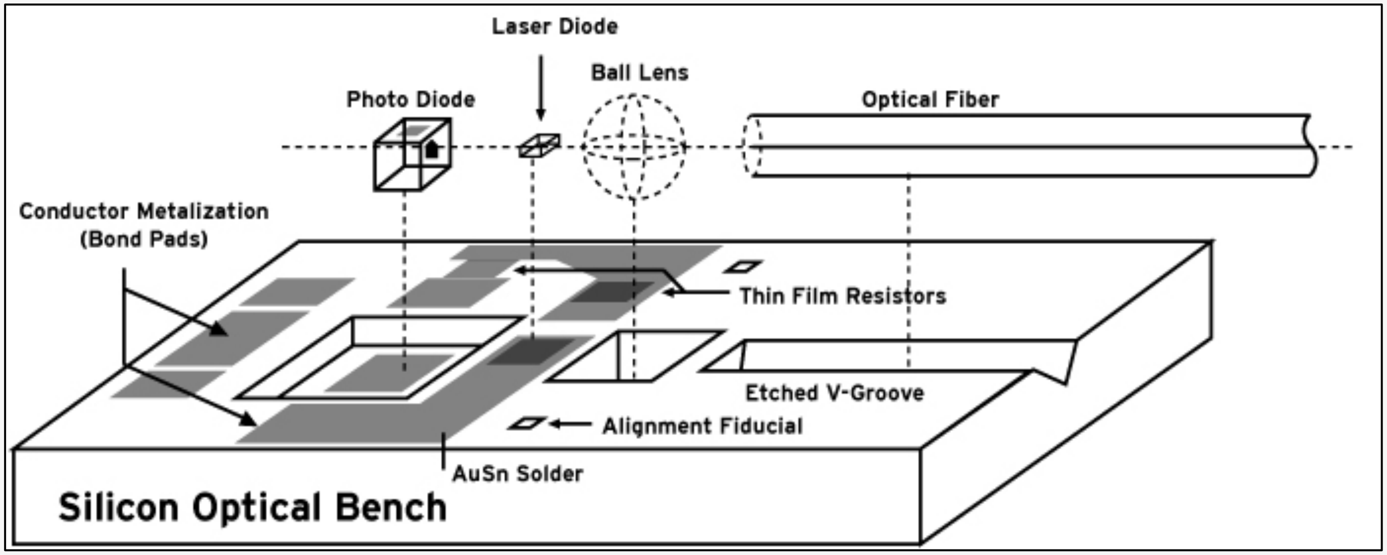
- World's Smallest MZI Modulator
- Extremely Efficient
  - $V_{\Pi}L_{\Pi}$ = 2 Volt*mm
- Mass Producible
  - 130 nm CMOS IC

PSMC

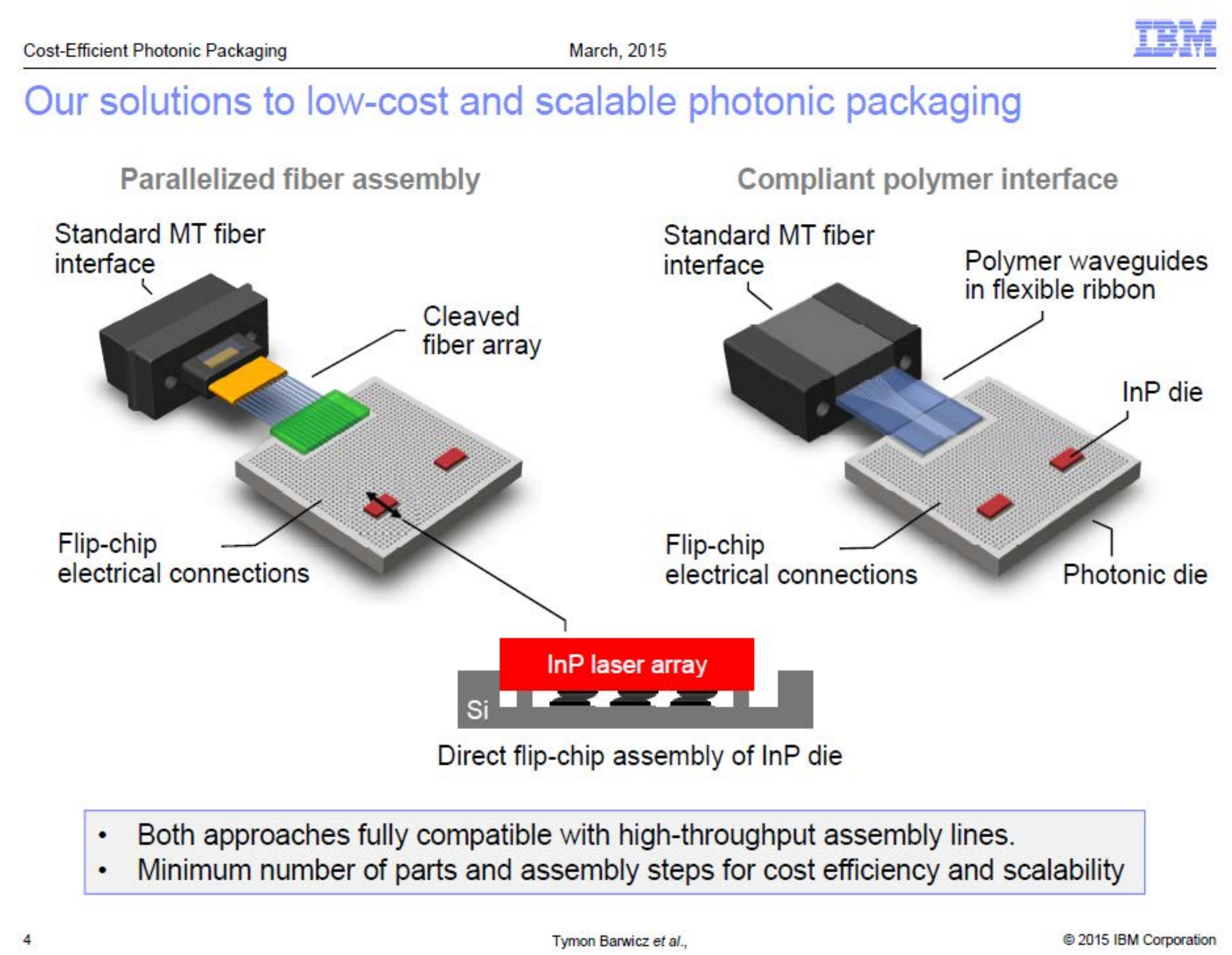
The silicon optical bench







How May/Will We Assemble These Devices ?

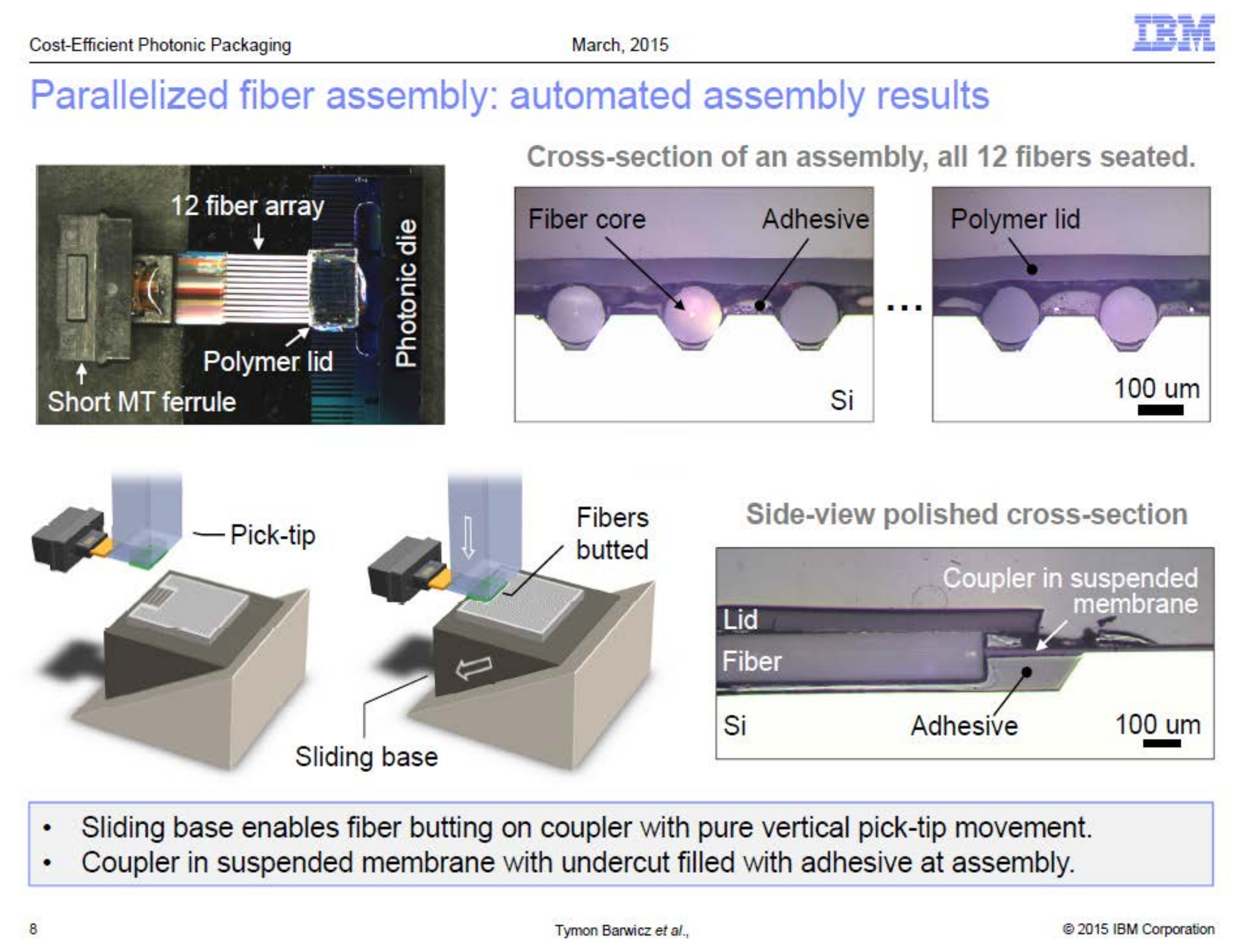


Our solutions to low-cost and scalable photonic packaging

Direct flip-chip assembly of InP die

- Both approaches fully compatible with high-throughput assembly lines.
- Minimum number of parts and assembly steps for cost efficiency and scalability

Tymon Barwicz *et al.*,



Cost-Efficient Photonic Packaging March, 2015 IBM

Parallelized fiber assembly: automated assembly results

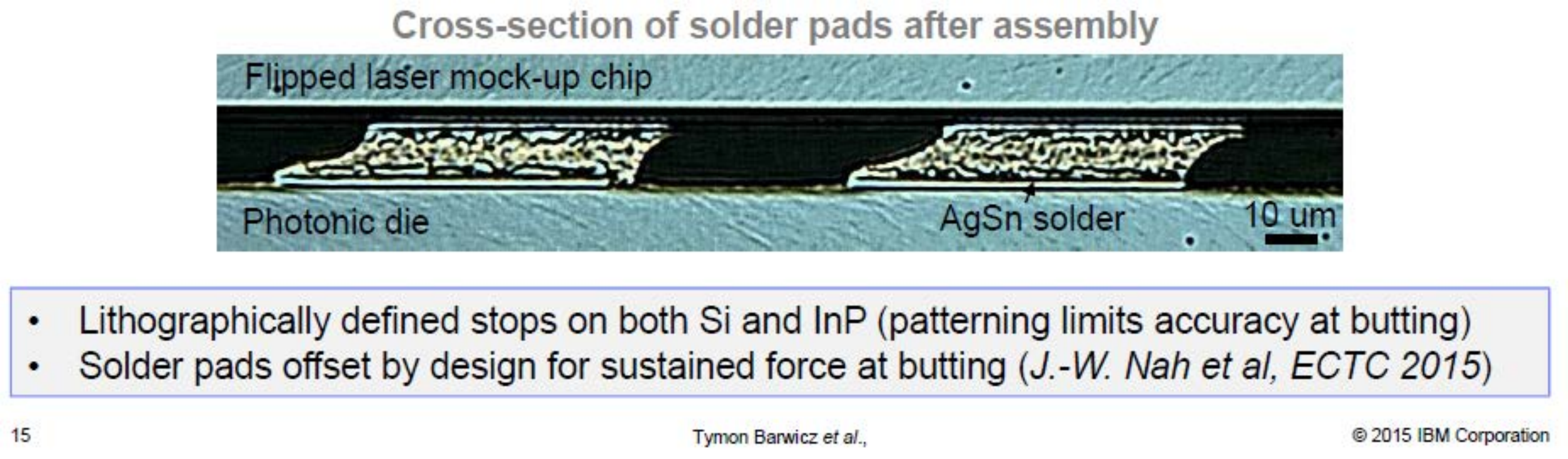
Cross-section of an assembly, all 12 fibers seated.

Side-view polished cross-section

- Sliding base enables fiber butting on coupler with pure vertical pick-tip movement.
- Coupler in suspended membrane with undercut filled with adhesive at assembly.

8 Tymon Barwicz *et al.*, © 2015 IBM Corporation

Capillary Action “pulling” Parts into Position



Cross-section of solder pads after assembly

- Lithographically defined stops on both Si and InP (patterning limits accuracy at butting)
- Solder pads offset by design for sustained force at butting (*J.-W. Nah et al, ECTC 2015*)

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Tymon Barwicz *et al.*,

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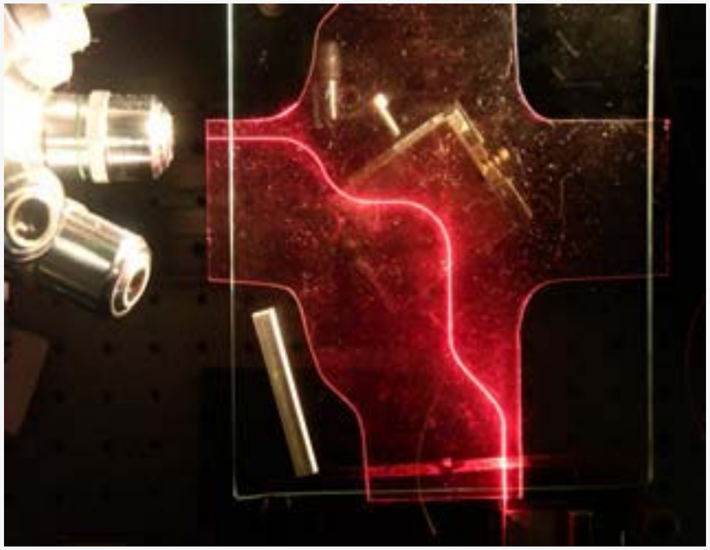
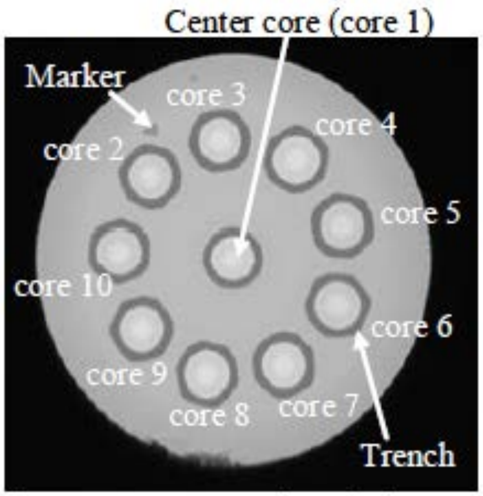
Emerging Capabilities





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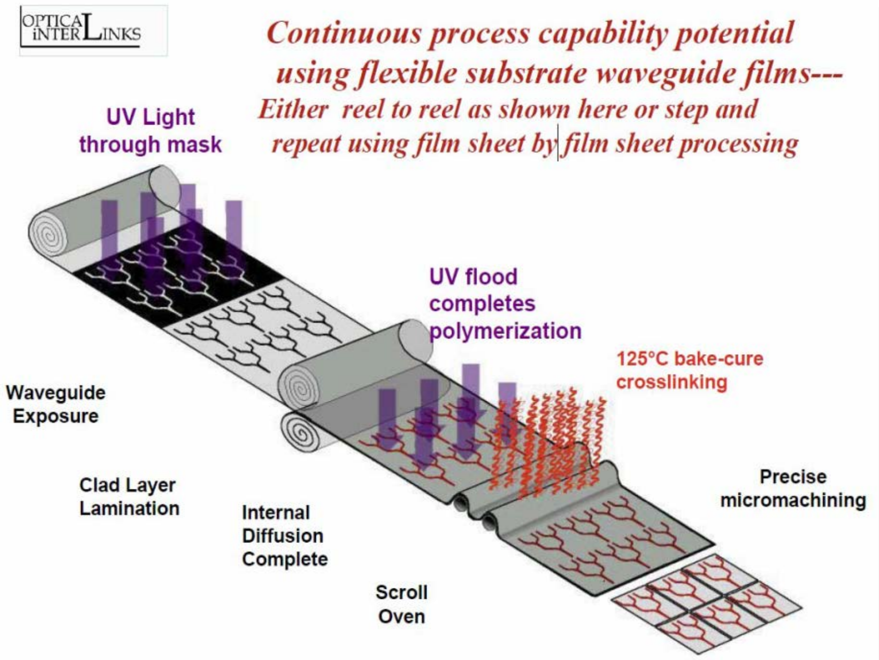
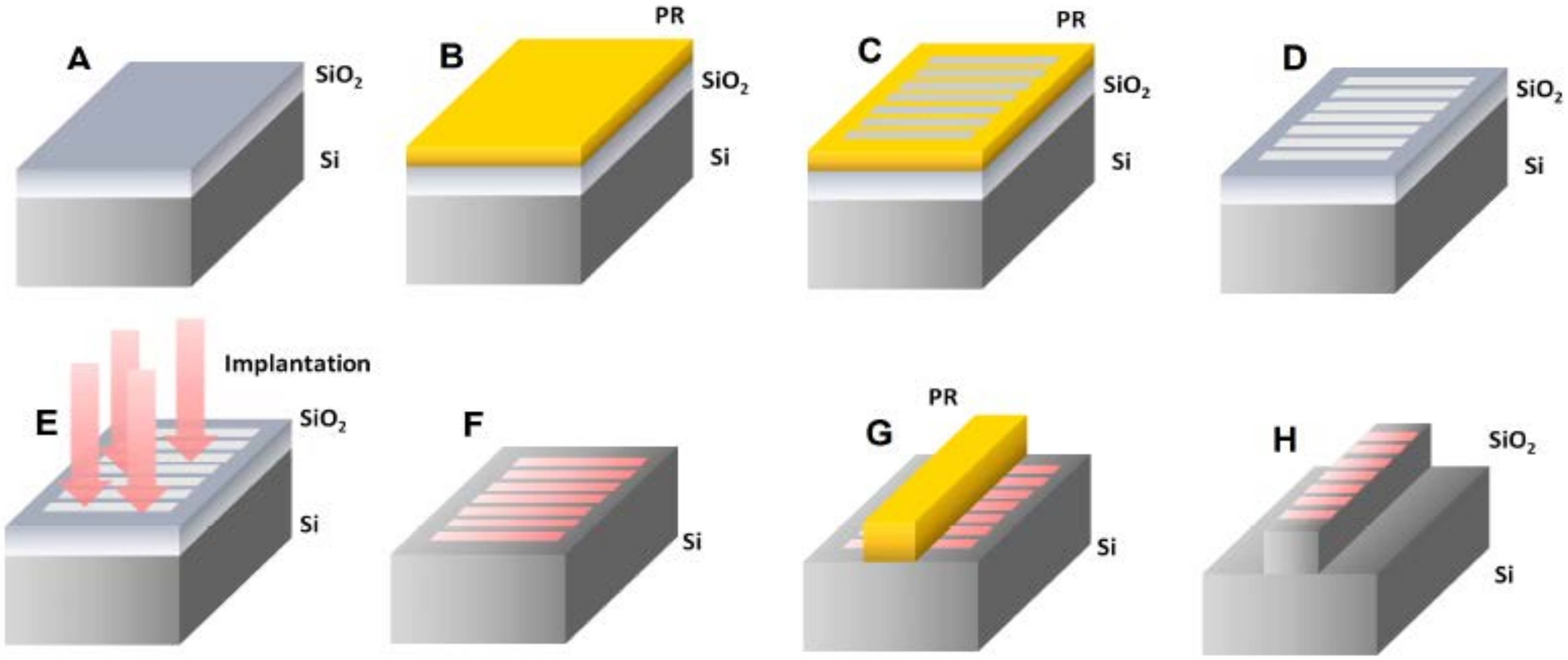


Continuous process capability potential using flexible substrate waveguide films---

Either reel to reel as shown here or step and repeat using film sheet by film sheet processing

Erasable gratings

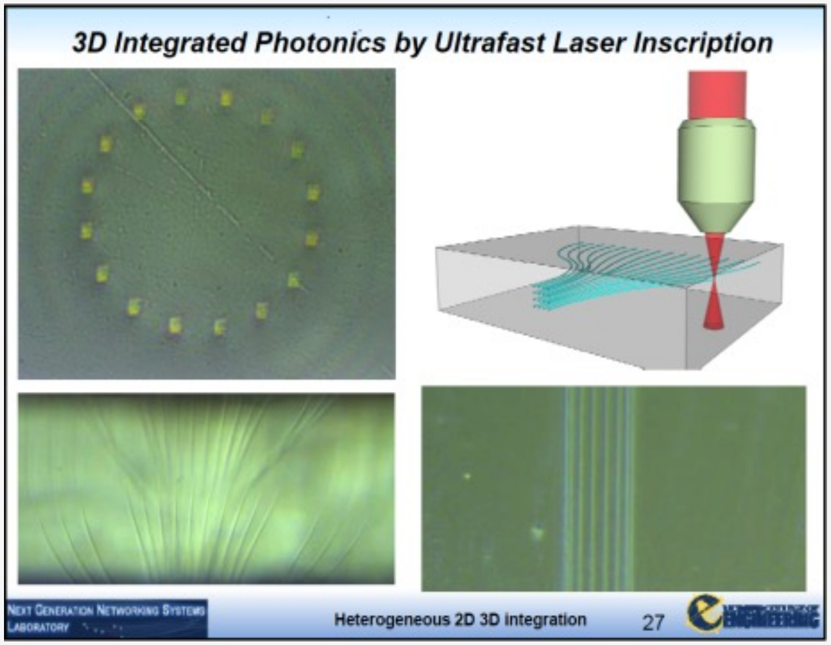
- Gratings formed by ion implantation rather than etching
- Formation of amorphous Si → refractive index change
- Annealing can repair lattice damage and therefore erase the grating



www.siliconphotonics.co.uk

Laser Waveguide Formation

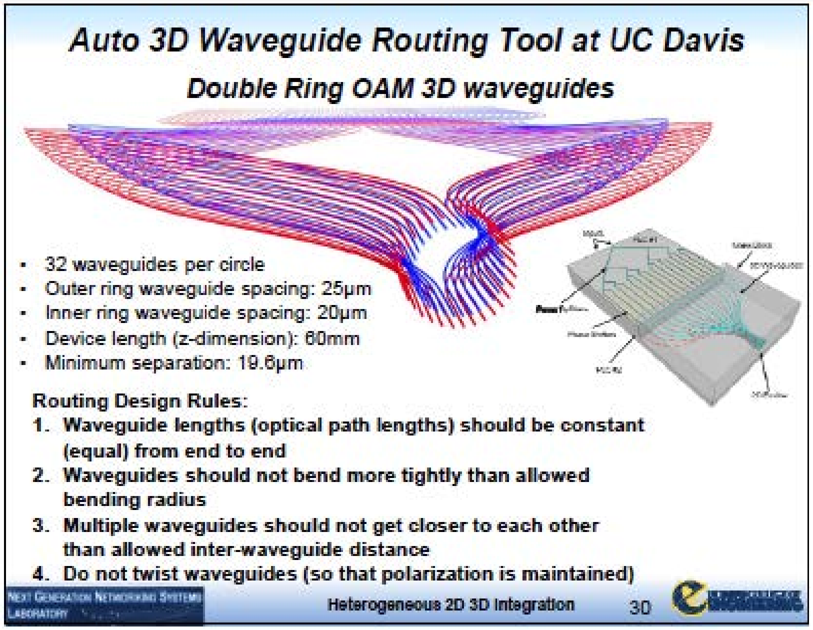
The graphics below are from the Yoo group at the University of California at Davis. This graphic illustrates inscribing waveguides within a bulk solid utilizing femoscecond laser pulses. Through the use of fiducials, cameras, high accuracy stages, careful measurement of parts and some complex software, waveguides can be accurately located within a bulk solid and used to fabricate a waveguide from one known point to another. Alternately, the process can be used to fabricate waveguide structures that are difficult to make utilizing other methods. For example, a structure such as a linear to circular transition can easily be fabricated.



3D Integrated Photonics by Ultrafast Laser Inscription

Next Generation Networking Systems Laboratory

Heterogeneous 2D 3D integration 27



Auto 3D Waveguide Routing Tool at UC Davis

Double Ring OAM 3D waveguides

- 32 waveguides per circle
- Outer ring waveguide spacing: 25μm
- Inner ring waveguide spacing: 20μm
- Device length (z-dimension): 60mm
- Minimum separation: 19.6μm

Routing Design Rules:

1. **Waveguide lengths (optical path lengths) should be constant (equal) from end to end**
2. **Waveguides should not bend more tightly than allowed bending radius**
3. **Multiple waveguides should not get closer to each other than allowed inter-waveguide distance**
4. **Do not twist waveguides (so that polarization is maintained)**

Next Generation Networking Systems Laboratory

Heterogeneous 2D 3D Integration 30

The process works because the laser pulses increase the index of refraction enough to make a waveguide. An inscription rate of 150 mm/sec. has been demonstrated making the

Designing Low Cost Optical Devices

Low cost, high performance optical products start with good design.

- Minimize the number of parts & assembly steps
- Utilize parallel, vs part-by-part, fabrication and assembly methods
  - panelize products
  - die to wafer bonding
  - wafer to wafer bonding
- Ensure the parts chosen have:
  - the necessary dimensional consistency
  - suitable location reference points
  - surfaces to which joints can be made
  - packaging that interfaces with assembly equipment
- Ensure the assembly process will be robust
  - evaluate part specifications and dimensional tolerances
  - maximize the tolerances required
- Ensure that dimensional requirements can be achieved by ensuring that:
  - fiducials and reference points are adequate
  - joining methods and materials are compatible with the dimensional and tolerance requirements
  - suitable assembly equipment is available

A Design Fundamental
Generalized Hooke's Law

$$\varepsilon_x = 1/E\,[\sigma_x - \nu(\sigma_y + \sigma_z)] + \alpha\Delta T$$

- This is the relationship between:
  - stress (σ_x)
  - strain (ε_x)
  - Young's modulus (E)
  - Temperature (T)
  - Poisson's ratio (ν)
- Determines the effect of temperature and stress on dimensional stability.

Simplified Hooke's Law

- $\varepsilon_x = 1/E\,[\sigma_x] + \alpha \Delta T$
- **Hooke's Law implies that material properties must be considered to provide stability over the product life.**
- **Ideal materials have high modulus & low thermal expansion and often provide a hermetic environment**
- **BUT these are expensive**
- **SO, use organic materials.**
- **BUT, organics have low moduli and high thermal expansion !! That's the Wrong Direction !!**

So, reducing cost by using organics requires careful, clever design.

The Accuracy Requirement

- Since the wavelength of light used is usually between 0.5 and 2.0 microns, mechanical accuracy and stability of 0.1, even 0.05 microns is needed.
- The expected product lifetimes are typically years in a variety of environments.
- The environments include temperature variations, mechanical shock and vibration and exposure to water and other potentially detrimental agents.

Perspective on the 0.05 micron Requirement

- **Typical optical devices have dimensions of 1 or 2 centimeters.**
- **The ratio on 0.1 micron to 1 centimeter is 1/100,000.**
- **Imagine a distance of 100 meters, a distance a little greater than an American football field.**
- **1/100,000 of 100 meters is 1 mm.**
- **So, we are talking about stability and accuracy comparable to the width of a blade of grass over the length of a football field !!**

Design Assessment For Low Cost and Performance

- **Are the locations on parts that need to be accurately located with respect to one another well defined by features the equipment can use as a reference ?**
- **Is the assembly equipment able to find the location of these critical points on the parts to be assembled?**
- **Is the equipment able to move the parts into position with respect to one another with the needed accuracy ?**
- If joining materials are used, will they adhere to the part surfaces ?
- **Will the joining temperatures and thermal profile distort the joint or parts irreparably ?**
- **Will all of the materials survive the assembly and operational environments and retain the desired location tolerances, especially during thermal cycling ?**

The Assembly Processes We Will Need

The Assembly Process

- **Assembly issues are addressed best when designing the product.**
  - **Select parts and joining methods that will provide the accuracy and stability required.**
- **Assembly requires bringing together the parts to be assembled.**
  - **Locating parts to be joined accurately and properly with respect to one another.**
  - **Forming permanent joints between parts with the accuracy required.**

Optoelectronic Assembly Methods

- Conventional surface mount assembly technology utilizing pick and place and reflow soldering.
- High accuracy placement and fastening utilizing suitable or specialized equipment.
- Laser welding
- UV cured adhesives
- Thermally cured epoxies
- Thermocompression bonding
- Wire bonding
- Brazing or soldering utilizing metallurgy that becomes rigid without cooling
- Flip chip assembly
- Dispensing of organic adhesives, encapsulants, underfills and adhesives
- Dispensing of optical joining materials such as UV cured adhesives that have good optical properties
- Assembly in particle free environments to minimize light scattering
- Testing utilizing methods to inject optical signals and/or detect them
- Optical components sometimes require assembly in the third, or Z, dimension where electronic assembly equipment is not suitable.

What Electronic Assembly Methods Provide Stability ?

- **Welding**
- **Solders**
  - **Off-Eutectic solders whose melting point increases on reflow**
  - **BUT Not Sn63 that cold flows**
- **High Modulus Organics**
  - **Epoxies**
  - **UV Cured Acrylates**
- **Thermocompression Bonding**
- **SiO_2 to SiO_2 bonding**
- **Others Known and To Be Determined**

The Written Chapter has more details on the materials and joining methods with an emphasis on achieving the sub micron tolerances required.

Assembly Equipment

Semiconductor Equipment Corporation

SEC 860 Specifications

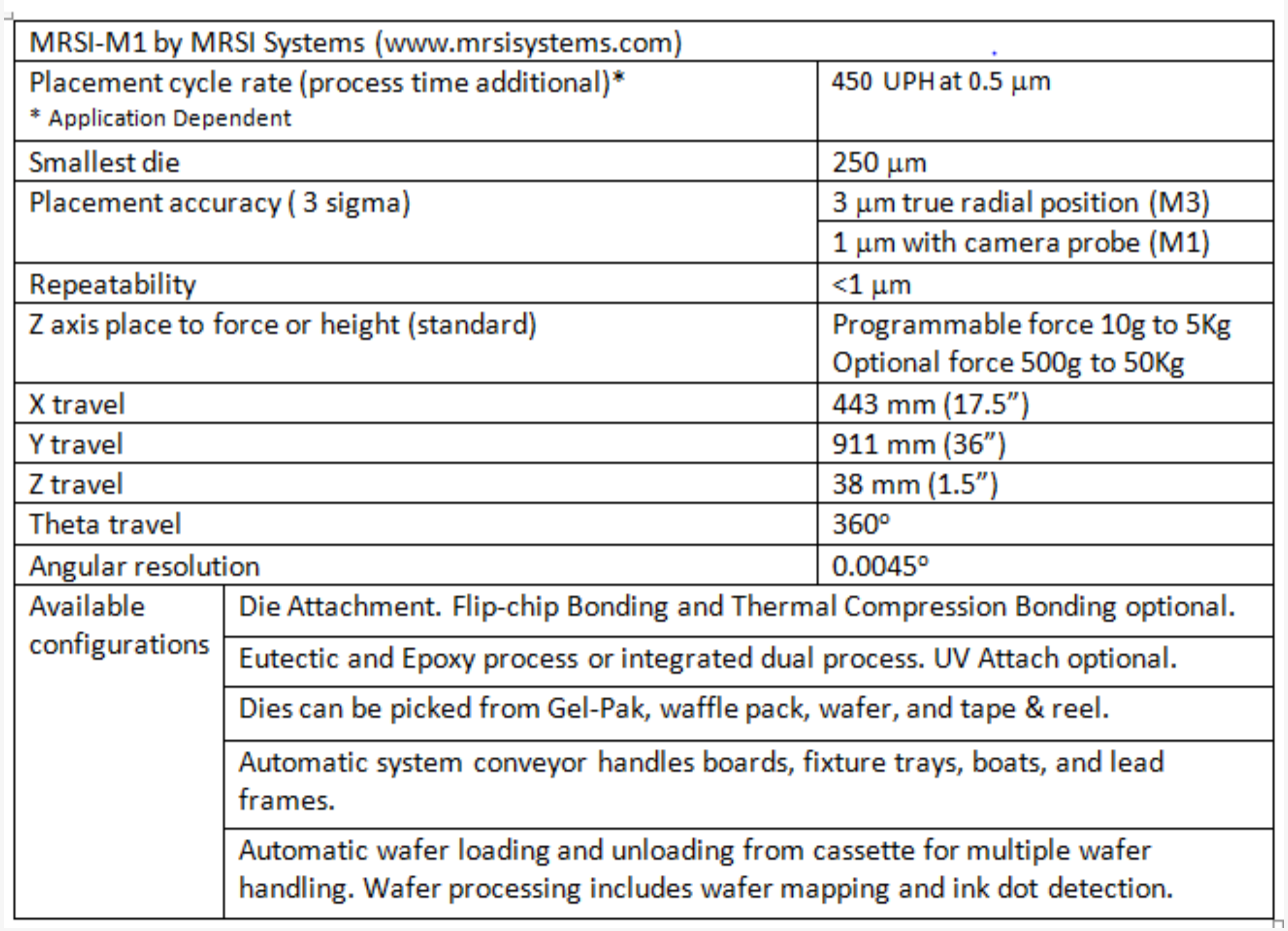
- High accuracy, within 1-2 microns
- Custom systems for your specific application
- Fast and easy set-up
- Compact footprint
- Intuitive Windows based operating system
- Low maintenance with minimal calibrations
- Select the options you need

Fine Tech
FINEPLACER sigma

Fine Tech FINEPLACER Sigma Specifications
0.5 micron accuracy
15 sec/placement + process time
Up 300 mm substrates
Up to 500 Newtons force
Attachment Methods

- Die Attach Film
- Gold-Tin Eutectic
- Gold thermocompression bonding
- Thermosonic bonding
- Solder Reflow
- UV cured polymers

MRSI Systems, MRSI-M-1



MRSI-M1 by MRSI Systems (www.mrsisystems.com)	
Placement cycle rate (process time additional)* * Application Dependent	450 UPH at 0.5 µm
Smallest die	250 µm
Placement accuracy (3 sigma)	3 µm true radial position (M3)
	1 µm with camera probe (M1)
Repeatability	<1 µm
Z axis place to force or height (standard)	Programmable force 10g to 5Kg Optional force 500g to 50Kg
X travel	443 mm (17.5”)
Y travel	911 mm (36”)
Z travel	38 mm (1.5”)
Theta travel	360°
Angular resolution	0.0045°
Available configurations	Die Attachment. Flip-chip Bonding and Thermal Compression Bonding optional.
	Eutectic and Epoxy process or integrated dual process. UV Attach optional.
	Dies can be picked from Gel-Pak, waffle pack, wafer, and tape & reel.
	Automatic system conveyor handles boards, fixture trays, boats, and lead frames.
	Automatic wafer loading and unloading from cassette for multiple wafer handling. Wafer processing includes wafer mapping and ink dot detection.

Palomar 6500 Die Bonder

Palomar 6500 Die Bonder Specifications

CYCLE TIME

Up to 1200 UPH

POST-PROCESS ACCURACIES

1.5 micron (post-eutectic bond)

PLACEMENT ACCURACY

3 micron, 3-sigma ultra-high accuracy eutectic
and
adhesive placements with cycle time of
approximately
3 seconds

K & S Thermocompression Bonder (TCB)

Chip to Substrate Bonder

APAMA™

Advanced Packaging with Adaptive Machine Analytics

Process Requirements	Specification 2015
Thin die handling (TSV 10:1) Die thickness	≥ 35 um
Fine pitch Cu Pillars Accuracy	± 2.0μ, ±20 mdeg, post bond (3σ) ±1.0μ, ±10 mdeg, glass die (3σ)
Cu Pillar Stacking Planarity	2μ / 10mm
High force capability	0.5 to 300N
Process Control Force Accuracy	0.25N or 1% (whichever larger)
Bond Line Thickness Z-Height Resolution	± 1.0μ (with temperature compensation)
Low COO – Productivity	Heat Ramp: > 200C/s
	Cool Rate: >100C/s
	Dry Cycle: <1.5 sec
	Sprint UPH: 3000 DH
Yield and Metrology	Die crack detection Contamination inspection Post bond overlay IR Align NCF

Placement Equipment Summary

Supplier, Model	Placement Accuracy, microns	Place Rate, UPH	Flexibility ↑	Cost ↓
Semiconductor Equipment Corp, SEC 850	+/- 1.0	~60		
Fine Tech, FINEPLACER sigma	+/- 0.5	240		
MRSI, MRSI-M1	+/- 0.5	450		
Palomar, 6500 Die Bonder	+/- 1.5	1200		
K & S, APAMA	+/- 1.0	<3000		

Test & Measurement

How Do We Test SiP Electronic-Photonic products ?

✓ **Integrate Optical Ports to Provide Access to Test Optical Functions**

- Optical Sources to Generate Test Light Beam

These Issues will be addressed in the Assembly and Test TWG Webinar November 17th but access must be part of package design and test engines must be incorporated into the package

- Coupling Methods
  - From/To Fiber/Fibers
  - From/To Waveguide/Waveguides
  - From/To “Free Space”

✓ **Mix with Electronic Test Points**

Optical Test Parameters, Values, Media and Ranges

Parameter	Range	Comment
Wavelength	650 nm to 1,700 nm	These are the primary wavelengths used for optical communications. Longer, and sometimes shorter, wavelengths are used in sensors and analytic applications.
Optical power	<1 watt (30 dBm). usually < 0.1 watt(20 dBm)	This value applies to most communications, sensor and analytic applications. Much higher power levels are used for industrial processes. Laser safety must be considered.
Wavelength spacing	Down to 25 GHz or ~0.2 nm at 1.5 microns	Applies in dense wavelength division communications multiplexing (DWDM) applications. More demanding in some sensors.
Optical Modulation Rate	<28 GHz near term, 100 GHz long term	This is the typical On-Off keying (OOK) single frequency, single polarization, single phase amplitude modulation rate.
Laser Sources	40 Gbs/channel and higher	Reliable laser sources for 40 Gbs/channel and higher rates utilizing higher order modulation are needed.
Optical Amplitude Modulation	Up to 32 levels (5 bit) per single phase near term, 1024 levels (10 bit) long term	Long term both the I phase and the orthogonal Q phase can be modulated with up to 1024 levels implying a spectral efficiency of 20 bits per hertz or 200 THz X 20 = 4000 Tbs/second on a single wavelength
Polarizations	2	Usually X and Y for SM. More complex for MM. Much more complex schemes are being explored.
Detectors	Responsivity	~1Amp/Optical watt (i.e. 1 milliamp with 1 milliwatt, 0 dbm of optical power.
Detector bandwidth	<28GHz near term, 100 Ghz long term	Going beyond ~50 GHz requires detectors ~ 1 micron in diameter resulting in complex challenges and maybe implementing plasmonic detectors.

Probing

# of simultaneous optical drive test signals needed	1 to 4 near term, up to 1024 long term	Some number of optical test signals may need to be injected into simultaneously into ribbon fiber or parallel optical waveguides with a combination of the following characteristics; one or more wavelengths modulated with controlled polarization, phase and/or amplitude with known and controlled skew between fibers.
Physical connections; Input of test signals and output of device signals	1. Conventional optical fiber connectors 2. Spliced fibers 3. Specialized for-test-only gratings built into substrates and products 4. Focused beams	A variety of probes (methods to get light into and out of optical ports, such as fibers, waveguides or elements such as lenses, mirrors, etc.) are likely to be required. For SM applications, alignment of the probes to the DUT (device under test) of < 0.5 microns, sometimes <0.1 microns will be required. MM applications require <5 micron alignment. Cleaning and inspection are required for each connector end contact face before mating with another connector to perform a test.
Test Detectors	Typically -30 dbm or higher, 650 nm to 1,700 nm, up to 50 Ghz	Need to measure power level, wavelength, polarization, latency and eye diagrams with up to 1024 signal levels (32 x 32 constellation). Also phase and skew between parallel signals.
Bit Error Rate (BER)	$< 10^{-9}$ to $< 10^{-12}$	BER is highly dependent on signal-to-noise ratio, signal conditioning, the application and the degree of error correction coding used, if any.

Measurements

MICRO-VU VERTEX MEASURING CENTER
AUTOMATED VISION FEATURES

- Powerful Machine Vision System
- New Systems are Probe Ready
- New Systems are Rotary Ready
- Programmable 6:1 or 12:1 Zoom Lens
- 42 Channel Lighting System
- "Mono-Rail" Bearing Design
- Fast, Accurate Z Measurements with Vision
  - Better than many laser systems
- Fast Servo Motor Control
- Two Sizes
  - 250 x 160 x 160 mm *from $32,600**
  - 315 x 315 x 160 mm *from $37,300**
  - 315 x 315 x 250 mm *from $41,300**

Offer resolution of 0.1 microns

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Key Attributes

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Assembly & Test Key Attributes

- Part placement, sec/part
  - For SM to <0.5 micron accuracy, sec/part
  - For MM to <5.0 micron accuracy, sec/part
- Number of parts
  - Degree of Integration; the more the better
- Assembly Equipment
  - Equipment Cost
  - Cycle Time for an Assembly
  - Part Joining time
  - Setup Time & Tooling Cost
- Optical chain movement during manufacture
- SM fiber attach to substrate, sec/joint
- Test time

Key Attribute Needs #1

Parameter	Metric	2013	2015	2017	2019	2025
Assembly	#REF!					
Single Mode Fiber attach to substrate	sec/joint	300	240	192	154	98
Single Mode Part Placement to <0.5 microns accuracy	sec/joint	20				
Multi-mode Fiber attach to substrate	sec/joint	300	240	192	154	98
Multi-mode Part Placement to <5.0 microns accuracy	sec/joint	5				
Package Costs	#REF!					
IC Package Cost	¢ per I/O	0.18	0.16	0.15	0.15	0.12
Package Cost (High Density Ceramic/w/ Area Connector)	¢ per I/O	5	4	3	2	1
Package Cost (High Density μvia Laminate w/ Area Connector)	¢ per I/O	4	3	2	2	1
Connector Cost	¢ per I/O	1.90	1.6	1.3	1	0.5
Energy Cost	$/Wh	0.40	0.30	0.25	0.20	0.10
Memory Cost (Flash)	$/MB	0.18	0.15	0.13	0.10	0.05
Memory Cost (SRAM)	$/MB	0.18	0.15	0.13	0.10	0.05
Cost of Test as a ratio to assembly	ratio	0.40	0.50	0.60	0.60	0.80
Cycle Time						
NPI Cycle Time	Weeks	20	16	12	6	3
Product Production Life (not including spares)	Years	7	6	5	3	3

Key Attribute Needs #2

Parameter	Metric	2013	2015	2017	2019	2025
Reliability						
Temperature Range	Deg C - Deg C	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 85
Number of Cycles	Cycles to Pass	1000	1000	1000	1000	1000
Vibrational Environment (PWB level)	G^2/Hz	0.03	0.03	0.03	0.03	0.03
Use Shock Environment	Gs & ms to Pass	50G (2ms)	50G (2ms)	50G (2ms)	50G (2ms)	50G (2ms)
Stability of Optical Alignment						
Devices	#REF!					
Number of stacked die (Max)	#	3	4	6	6	9
Number of Die in SiP (max)	#	6	7	7	9	12
Electrical & Test						
Frequency on Board	MHz	10K	25K	40K	100K	1000K
Impedance Tolerance	%	7	7	5	5	3
Number of Voltages	#	10	10	12	12	14
Off Chip Driver Rise Time	V/ns	25	30	35	50	100
Serial Bus Rate (1 bit)	Gb/s	8	10	14	24	40
Built In Self Test (BIST)	%	50	70	85	90	95
Boundry Scan	%	20	35	50	75	85
Test pad access minimum	%	25	20	15	5	3
Maximum escape rates	DPMO	500	400	300	200	100

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Needs and Gaps

Assembly & Test Technology Needs (< 5 Years)

- Design software able to utilize Hooke's General Law over temperature to ensure designs will function over the life of the product.
- Properties of standard materials for use in design.
- Training of designers in Design for Manufacturing to reduce Cost
- Standardization
  - Platforms and parts
  - Sensor packaging
  - Transceivers
  - Process Design Kits (PDK)
  - Test interfaces
- Metal to metal, epoxy, or alternate joining methods that are fast and stable over the life of the product.
- Self-alignment/passive alignment methods.
- Improved machine interfaces to minimize programming and set-up time to reduce costs for short optical product runs.

Material Properties Needs

- Detailed Properties of some materials, especially organics, is not readily available. Manufactures provide data sheets
  - Must provide Material Safety Data Sheets (MSDS)
  - Data sheets exclude properties needed for optical design.
- Properties needed include:
  - Young's modulus vs temperature, both before and after curing
  - CTE vs temperature
  - Poisson's ratio
  - Dielectric constant & loss tangent vs frequency up to 100GHz, etc.
    - vs water content & temperature
  - Dimensional change from water content

The Industry needs to develop standard sets of needed material properties and manufacturers then need to routinely provide that data.

Assembly & Test Technology Needs (> 5 Years)

- Light sources that can be modulated at 50Ghz+ compatible with CMOS
- ntegrated devices to minimize part count and the need for assembly
- Optical Assembly equipment customized for
  - Tight tolerances
    - Placement
    - Joining Methods
  - Rapid set up
  - Able to Handle “odd” form factor, non planar parts
- High tolerance substrates/platforms that Optical Components are assembled on.
- Low cost, optical components with sub micron tolerances
- Methods to simulate manufacturing processes to enable more rational selection of materials, processes and equipment
- Components that provide improved functionality per unit volume. (i.e. smaller demultiplexers)
- Erasable optical ports to temporarily put optical probe test points on a chip.

Assembly & Test Gaps

- Optically capable assembly equipment with low setup and tooling costs.
- Low speed of assembly, test and other process equipment that results in high costs
  - Joining processes with long cure/joining/cooling cycles that raise cost
  - Limits resulting from adopting existing equipment, materials and methods to optical assembly and test
- Difficulties building in the Z dimension often required by optical devices
- Limited availability of manufacturing simulation tools and software
- Elimination of component attach processes that allow micro motion such as creep with epoxy during the curing step
- Difficulty eliminating Active Alignment
- Cost of Test Equipment

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Potential Solutions

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Potential Solutions for Assembly & Test # 1

- Provide more comprehensive material properties.
- 3D print optical parts/benches/substrates/ platforms with >0.1 micron accuracy that optical elements can be assembled on.
- Better software interfaces to existing and new Equipment.
- Assembly Equipment specifically intended for Optical Products:
  - Accurate to < 1 micron and 6 dimension accuracy
  - Rapid set up
  - Tight tolerances

Potential Solutions for Assembly & Test # 2

- **Utilize laser processing to:**
  - **make optical waveguides in-situ**
  - **Nano-machine parts and optical structures.**
- **Utilize electron/ion beam based equipment for measuring, and nano finish machining.**
- **Utilize Monte-Carlo and adaptive design methods for meta structures and improved materials.**
- **Utilize plasmons to minimize size and maximize functionality.**
- **Utilize higher levels of integration, more functions per unit volume.**

1 cubic mm has ~ 10^{20}atoms.

What can be done with that ?

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Show Stoppers

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Assembly & Test Show Stoppers

- **Continuing improvement in electrical methods keeping that technology less expensive than optical solutions**
- **Achieving low cost heterogeneous assembly of III-V parts with CMOS devices.**
- **Inability to utilize materials or processes due to environmental related constraints (RoHS, REACH, WEEE, etc. TBD)**
- **High costs resulting from low production volume due to lack of optical applications and standards**

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Next Steps

- We Anticipate Having Workshops for the PSMC TWGs and Emulators at the December ’15 Cambridge Meetings.
- Plan on Participating to Comment, Validate, Improve the chapters.
- All of the Workshop Results Will not Make it into the Written Roadmap, so attend to Maximize Your benefit and contribution.
- See you in a Few Weeks !

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CLICK HERE TO SEE THE WEBINAR RECORDING

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