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Photonic Systems Manufacturing Consortium

Define the difficult challenges.
Create the potential solutions.

Photonic System Packaging Roadmap

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PSMC-AIM Photonics Webinar Series

November 3, 2015

http://photonicsmanufacturing.org/

Packaging TWG Charter

Address the technology gaps and challenges that are limiting the advance of hardware technology for use in heterogeneous integrated electronic-photonic systems manufacturing.

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Our Roadmapping Process

The Roadmapping Process

Goals and Objectives

✓ Provide a 15 year Roadmap of key packaging requirements for heterogeneous integrated photonic/electronic systems

✓ Identify gaps and difficult challenges that must be overcome to meet Roadmap requirements

✓ Identify potential solutions where possible

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Product Emulators Used As Packaging Drivers

Data Center Emulator Grand Challenges:

- ✓ Photonic integration for bandwidth density
- ✓ High-volume manufacturing to meet system demands and cost objectives.

IoT Emulator Grand Challenges:

- ✓ Low Bandwidth, “High” Latency, Low Power – Primarily E to O,
- ✓ The Plethora of consumer, industrial, medical and military applications.

Packaging is a key enabler for addressing the grand challenges of both emulator Groups.

Component level photonic packaging will continue to make progress but it can not contribute much to the revolutionary changes required to meet 15 year requirements

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Photonic Packaging Includes Component level and Heterogeneous Integration Level Packages

In The Roadmap Photonics Includes:

- ✓ Optical to electrical conversion
- ✓ Electrical to optical conversion
- ✓ Optical switching
- ✓ Optical sources
- ✓ Optical detectors
- ✓ Optical modulators
- ✓ Photonics as sensors are part of IoT emulator requirements

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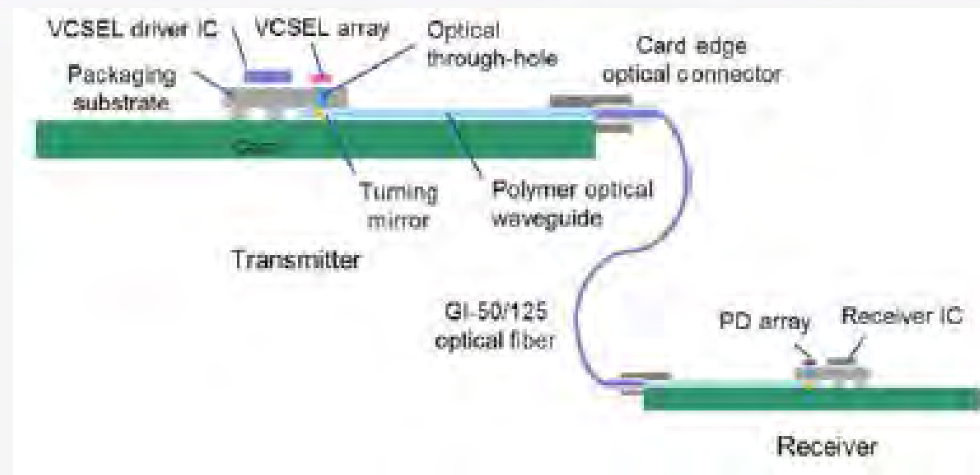
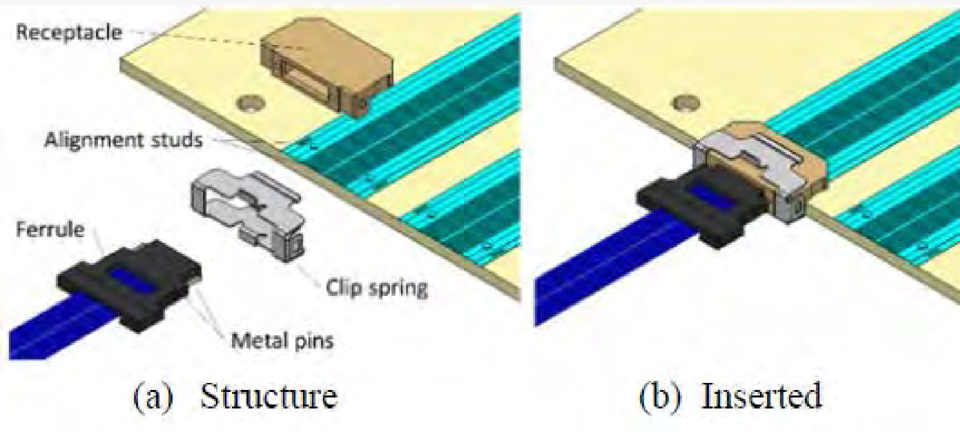
Today's Component Level Photonic Packaging

Current Technology

Diagram of the on-board optical interconnect





(a) Structure (b) Inserted

Card edge connector

Assembly rather than parallel manufacturing does not meet future requirements for cost, size.

OK for board but not for package

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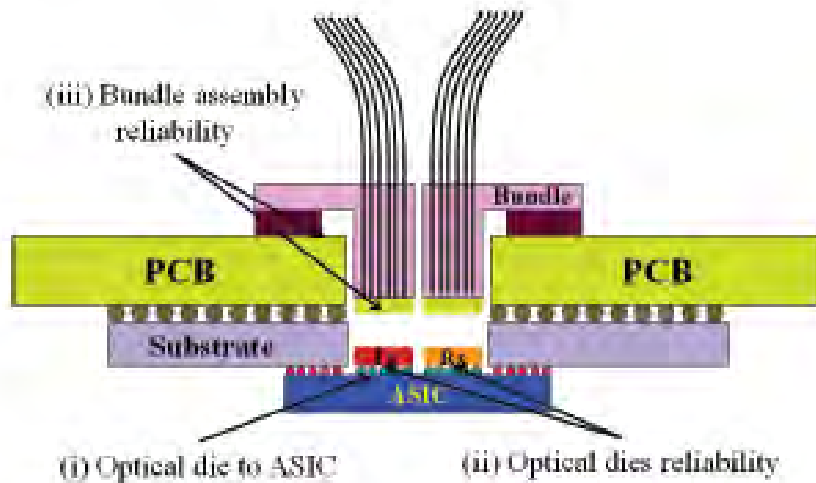
Near Term Component Level Photonic Packaging

Current Technology

Multi- channel optical interconnect



Module technology for very high density high speed data.

Next level of integration is a single integrated package incorporating a 2.5D electronic/photonic package substrate.

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Photonic Component Packaging Challenges

- ✓ Low cost
- ✓ High reliability
- ✓ Use available equipment
- ✓ High bandwidth per channel
- ✓ Small size
- ✓ Low power

Near term the Roadmap is known or can be generated without significant research

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Situation Analysis for Electronic-Photonic Systems Packaging

Driving Photonics Manufacturing

Situation Analysis

- ✓ The requirements are rapidly changing for data transmission, storage and processing.
- ✓ These changing requirements are driving revolutionary changes after 50 years of Moore's Law scaling with change that was largely evolutionary.

Environmental Changes

- ✓ We are approaching the end of Moore's Law scaling
- ✓ The emerging world of the internet of everything causing explosive growth in the need for connectivity
- ✓ Mobile devices like smart phones and tablets are growing rapidly in number and data requirements driving explosive growth in the required global network capacity
- ✓ Migration of data, logic and applications to the cloud drives demand for reduction in latency while accommodating the global network capacity growth
- ✓ The development of Wafer Level packaging (WLP), 2.5D and 3D integration techniques for packaging

Requirements To Support The Expanding Data Traffic

Over the 15 year life of this roadmap we must change the global network, the components in it and most of the elements attached to meet the requirements

- ✓ Improve power efficiency by 10^4
- ✓ Improve cost per function by 10^4
- ✓ Increase the number of network ports by 10^6

All this is needed at *no increase in total cost*

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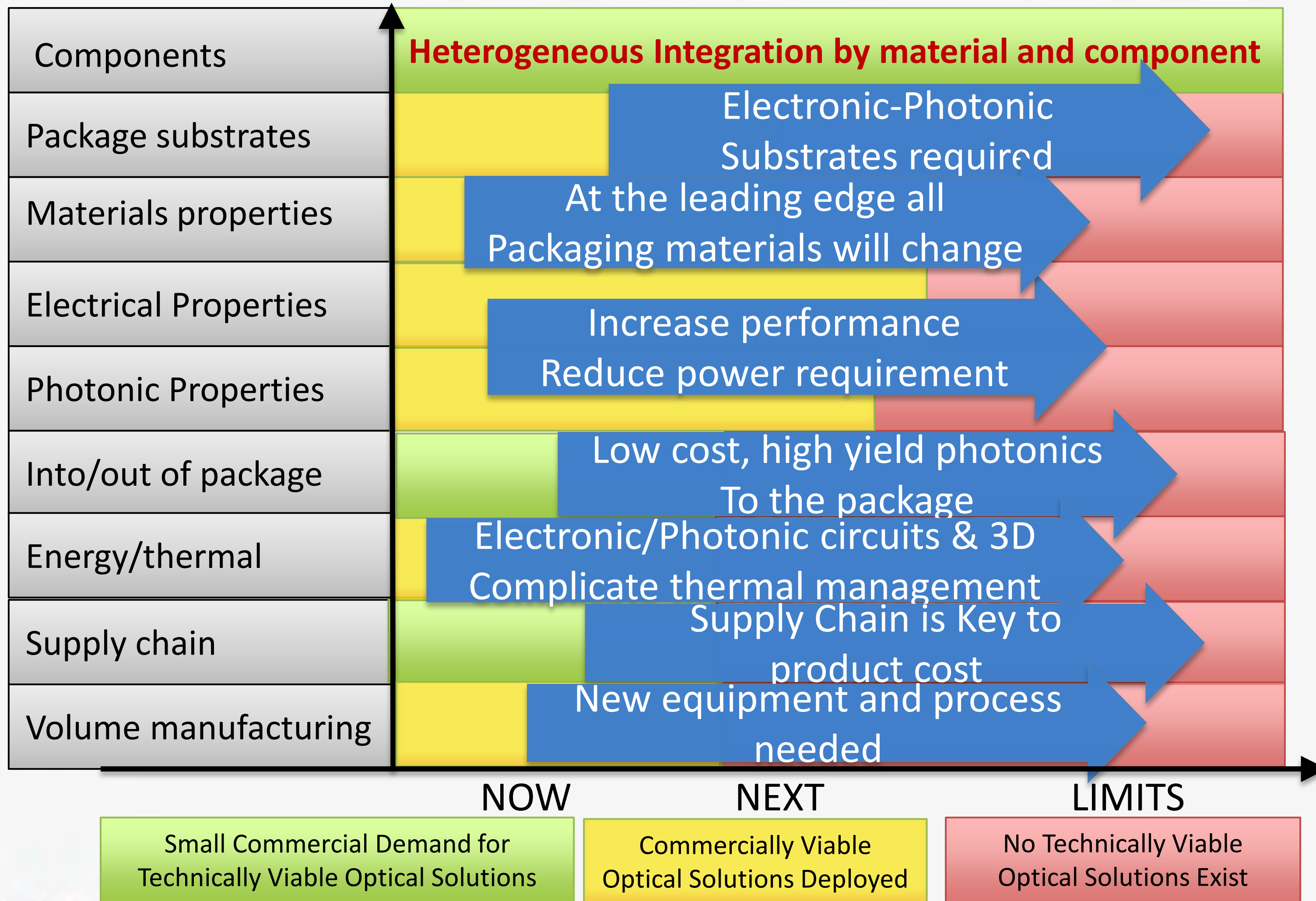
Photonic System Packaging Roadmap



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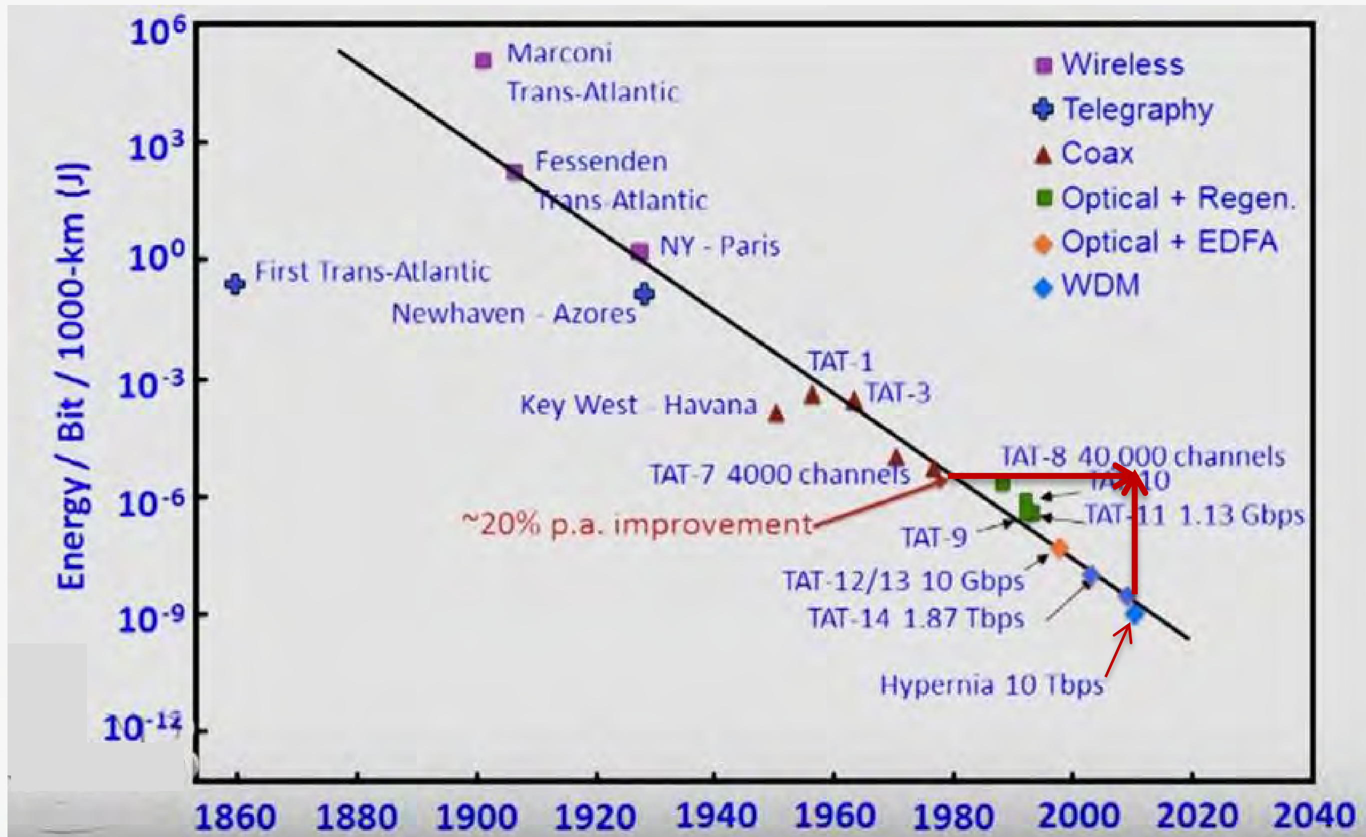
The Promise Of Silicon Photonics

- ✓ Making photonic integrated circuits on silicon using CMOS process technology in a CMOS fab
  - – Reduced Cost
  - – Reliable proven processes for all electronic components
  - – Low power processes
- ✓ Move Photons Closer to the transistors
  - – Reduced cost, latency and power

Photonics Enables Power Reduction

A Reduction of ~1,000,000X in 30 years



Source: UCSB

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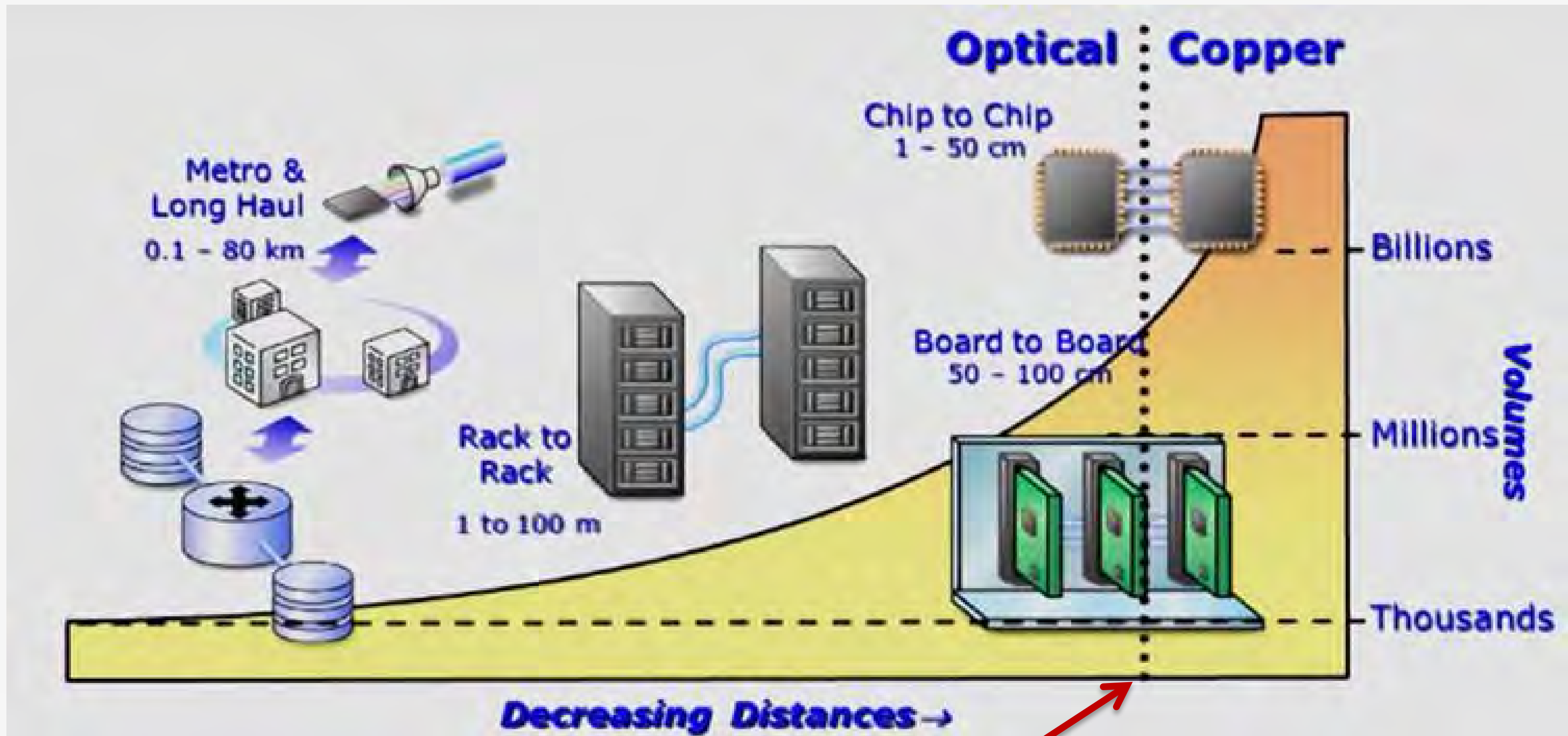
Key To Power, Bandwidth Density and Latency
Move the photons closer to the transistors



We are here today

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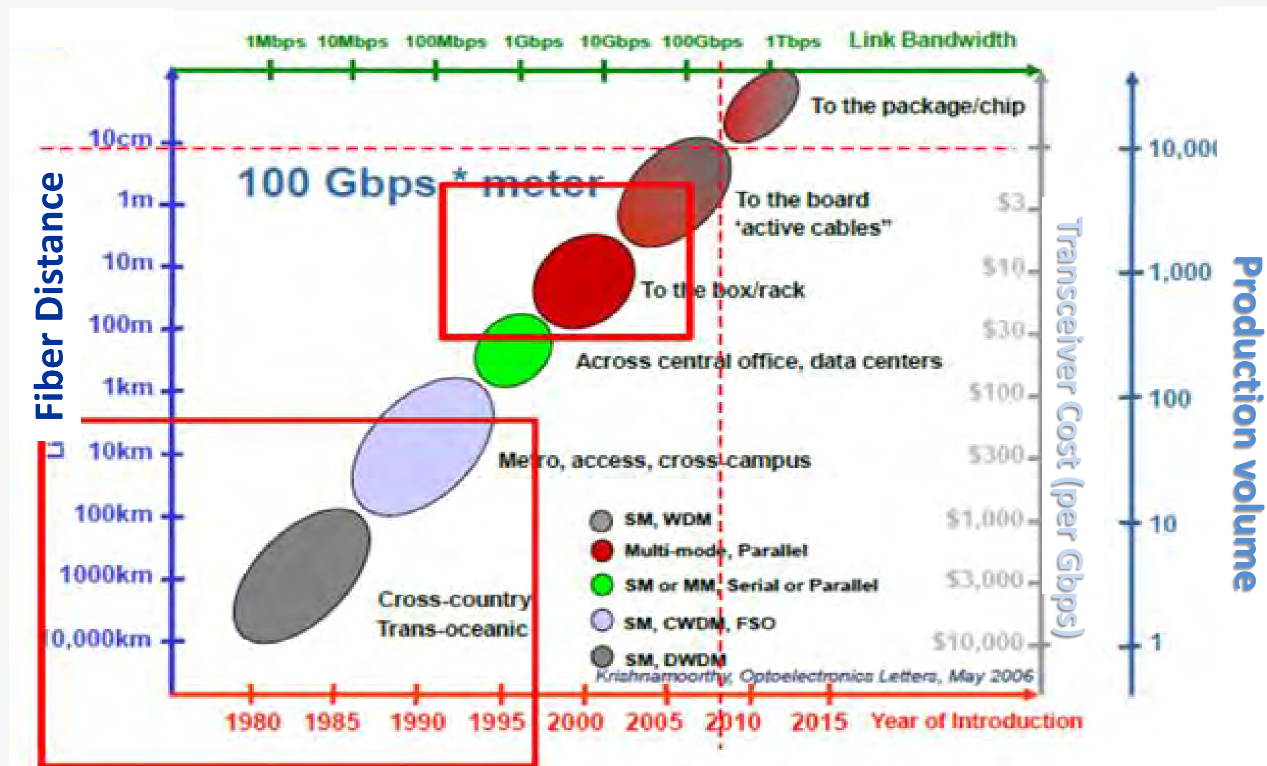
Move The Photons Closer To The Transistors

As Photons reach the package unit volume expands rapidly driving down cost



Source: Brocade

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Packaging Requirements

- ✓ **Protect the contents from damage**
  - Mechanical
  - Chemical
  - Electrical
  - Thermal

Photonics may be in environments we don't contemplate today as photons get closer to the transistors in an IoT world.

- ✓ **Provide power for operation**
- ✓ **Provide data input/output connections**
- ✓ **Do no harm**
  - Latency
  - Power
  - Cost
  - Reliability

In many of these parameters packaging is the weak link

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Data Center Packaging Requirements

The Data Center Today

The pictures you don't usually see

Water storage tanks

Water Vapor/Steam from refrigeration

Chilled water

Return water

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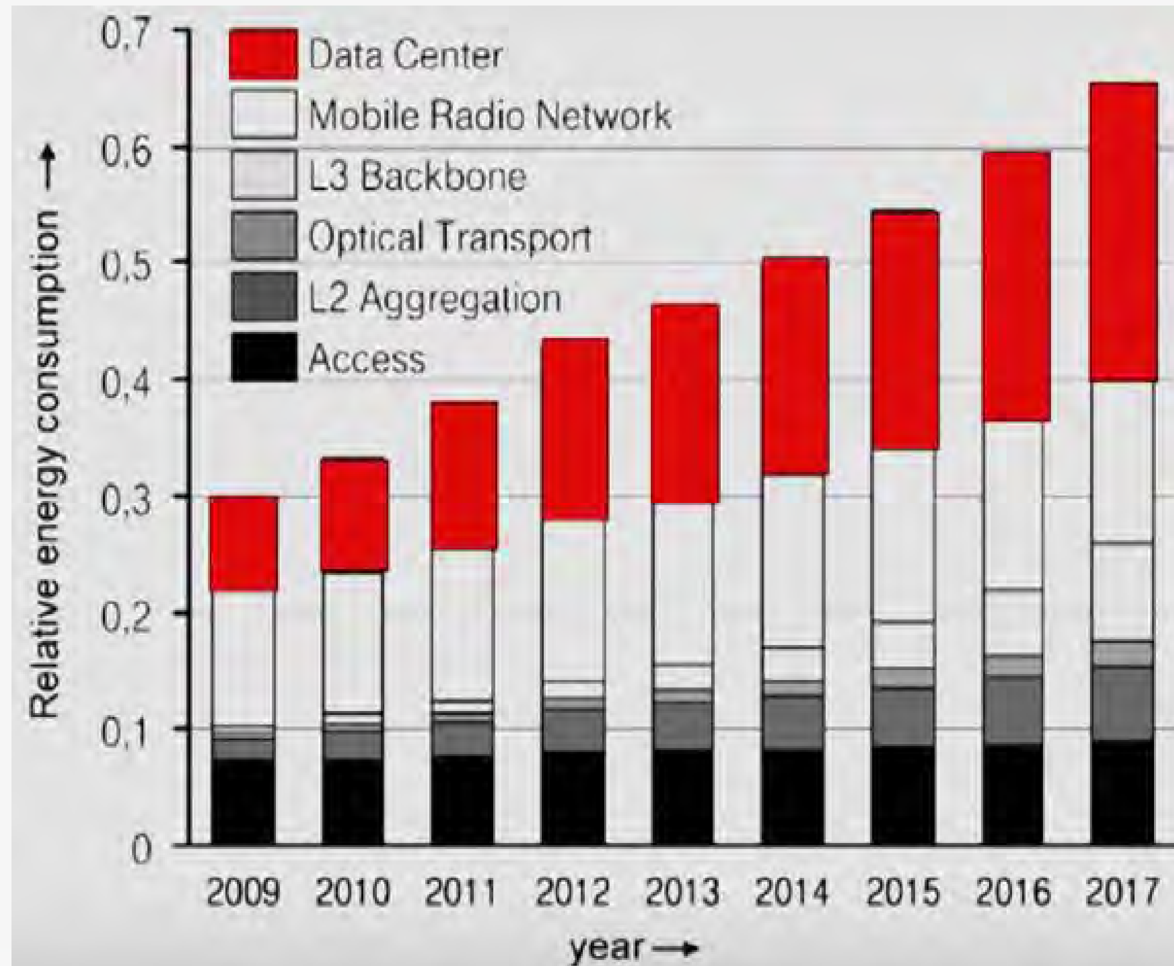
Power Consumption Is A limiting Factor And Packaging Plays A Major Role in Power

The Data center power percentage is growing



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Performance Requirements To Support The Roadmap View Of The Future

- ✓ Higher bandwidth density
- ✓ Lower latency
- ✓ Increased data processing speed
- ✓ Expanded data storage
- ✓ Ensured reliability
- ✓ Improved security

all at no increase in cost

Performance Requirements To Support The Roadmap View Of The Future

- ✓ **Higher bandwidth density**
- ✓ **Lower latency**

Each of these requirements pose difficult packaging challenges

- ✓ **Improved security**

all at no increase in cost

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Potential Solutions For These Difficult Challenges

Driving Photonics Manufacturing

Potential Solutions To Support The Roadmap View Of The Future

- ✓ Higher bandwidth density

WDM single mode Photonics to the package

- ✓ Lower latency

Flat photonic network- replace tree architecture

- ✓ Increased data processing speed

Increased parallelism- more cores & software to match

- ✓ Expanded data storage

3D memory, expanded bus width, hierarchical architecture

- ✓ Ensured reliability in a world where transistors wear out

Intelligent redundancy

Continuous test while running

Dynamic self repair

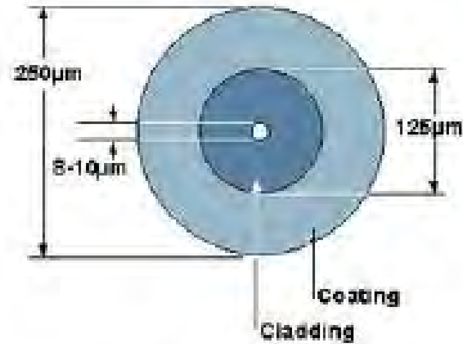
Graceful degradation

- ✓ Improved security while maintaining process speed and latency

Hardware and software combined-distributed over the global network

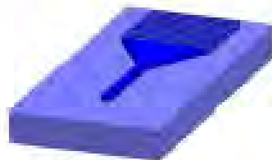
Optical Coupling Remains A Difficult Challenge

TYPICAL MULTIMODE CROSS-SECTION

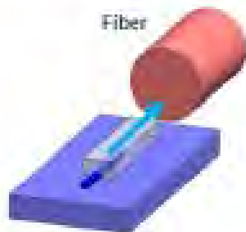


TYPICAL SINGLEMODE CROSS-SECTION

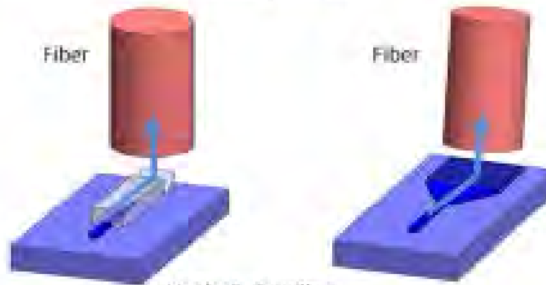
Spot Size Converter



Grating Coupler



Horizontal Coupling



Vertical Coupling

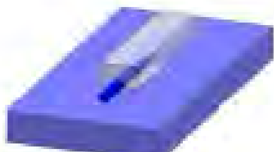
Optical Coupling Remains A Difficult Challenge

***Time is money*:**

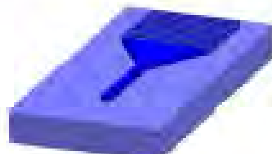
New low cost, small size, self aligning coupling technology will be essential

TYPICAL MULTIMODE CROSS-SECTION

TYPICAL SINGLEMODE CROSS-SECTION



Spot Size Converter



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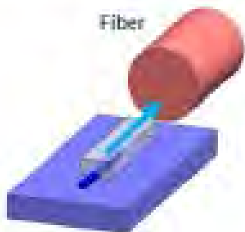
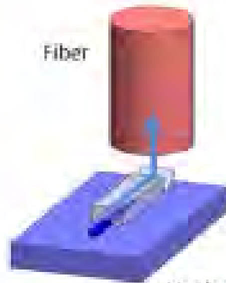
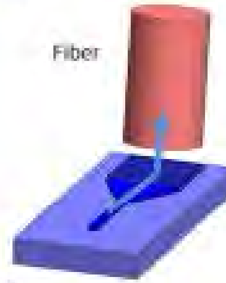
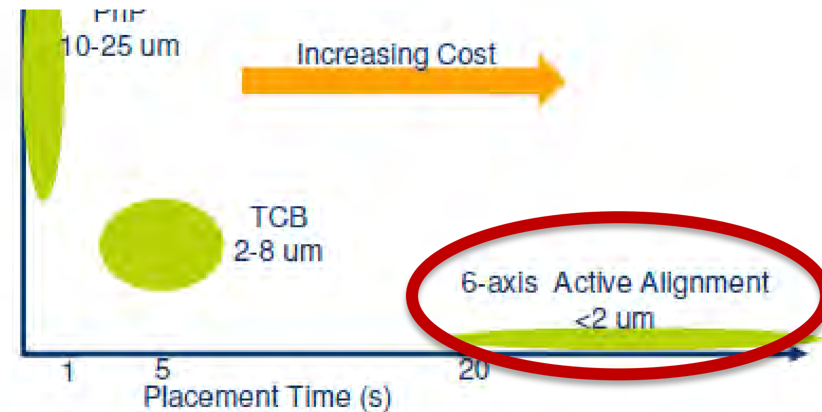


Horizontal Coupling





Vertical Coupling



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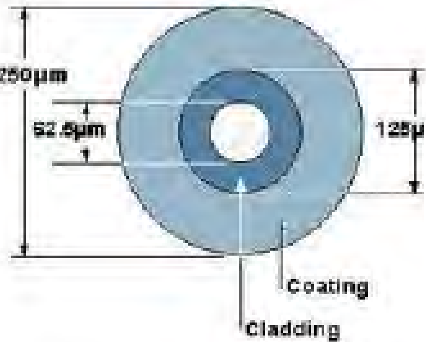
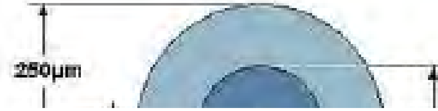
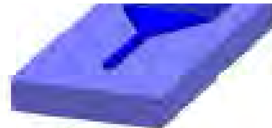
Optical Coupling Remains A Difficult Challenge

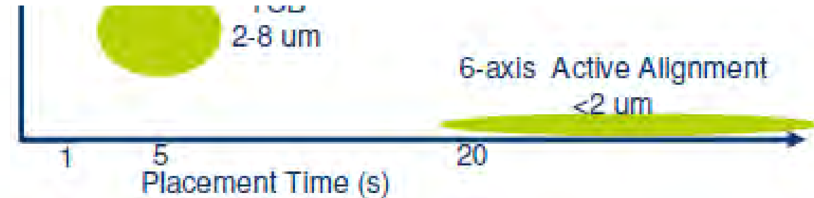


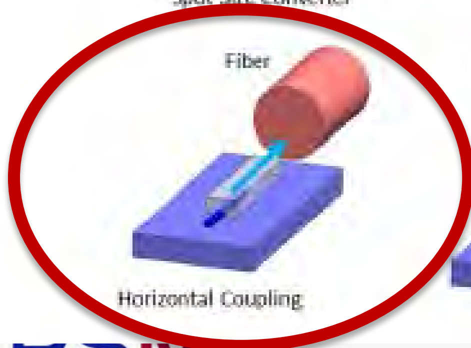
TYPICAL MULTIMODE CROSS-SECTION

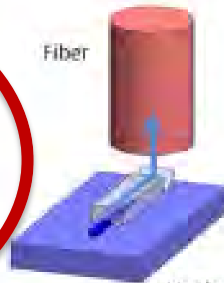


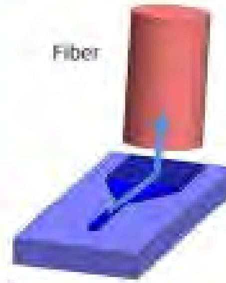
For Heterogeneous Integration edge coupling will be the solution since the top must be committed to thermal management











Vertical Coupling

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A Revolutionary Change In Packaging Is In Process

"Heterogeneous Integration in 3D Photonic/Electronic SIP"

Driving Photonics Manufacturing

A Revolution in Packaging Is Needed To Address Data Center Packaging Challenges

At the leading edge everything will change to allow high reliability SiP products meeting market needs at low cost.

This requires:

- ✓ New design and simulation tools
- ✓ New materials
- ✓ New device designs and architectures
- ✓ New package architectures
- ✓ New network architectures
- ✓ New manufacturing processes

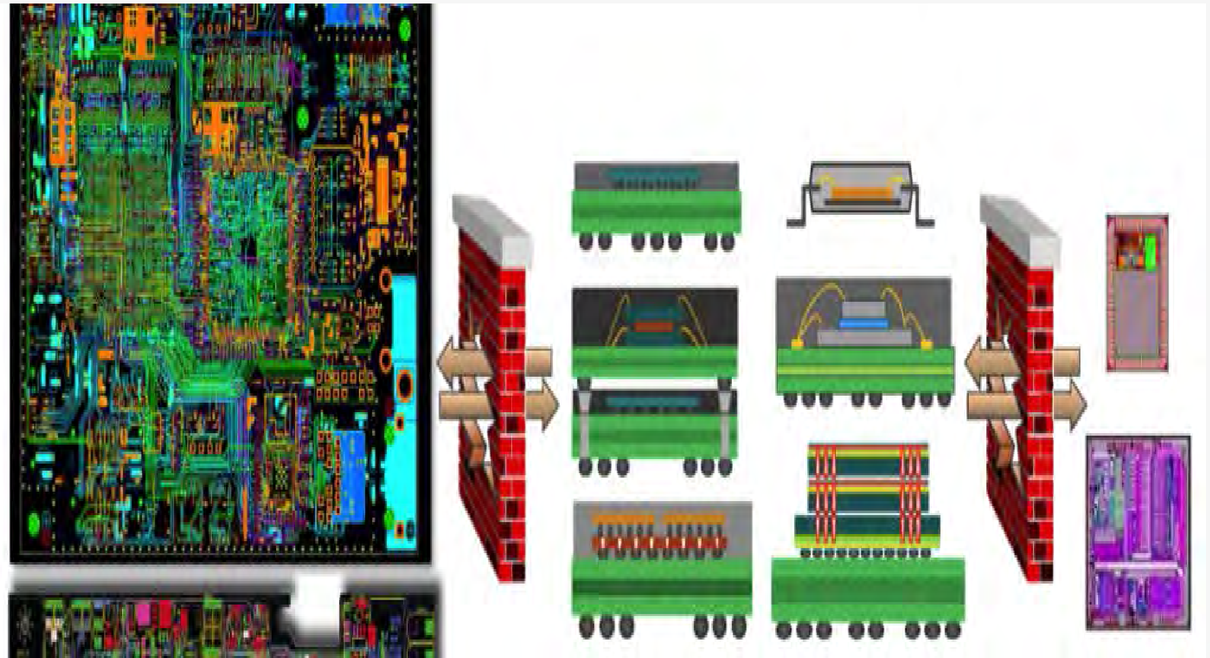
Co-design and Simulation Tools for SiP

New CAD tools for heterogeneous integration across boundaries of device, package, printed circuit board and product essential to migration to higher density (SoC, SiP, 2.5D, 3D, etc.) and time to market.

Electronics – Photonics – Plasmonics

This enables:

- ✓ Increased performance and bandwidth
- ✓ Decreasing latency, power, size, cost
- ✓ Reduced time to market



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Spice modeling Of Electro-Optical Photonic Circuits

SPICE modeling could include the effects of dispersion, fiber attenuation, and total delay. Such a model could be used to simulate signal integrity for optical/electrical links using a familiar platform.

Integrated simulation and design tools are needed to reduce cost and time to market for SiP addressing electronics, photonics and plasmonics.

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Spice modeling Of Electro-Optical Photonic Circuits

SPICE modeling could include the effects of dispersion, fiber attenuation, and total delay. Such a model could be used to simulate signal int
fa

Move the experiments and design iterations to the computer

Integrated simulation and design tools are needed to <u>reduce cost</u> and <u>time to market</u> for SiP addressing electronics, photonics and plasmonics.

Co-Integration of Technologies

Use each technology where it is the best:

- ✓ Electronics
  - Active logic and memory (Processing and routing)
  - Smallest size
- ✓ Photonics
  - High bandwidth
  - Energy efficient
  - Long and intermediate distance
- ✓ Plasmonics (R. Zia et al., “Plasmonics: the next chip-scale technology”, Materials Today 9(7-8), 2006)
  - Much smaller than photonic components
  - Potentially seamless interface between Optics and Electronics
  - Low power active functions

Heterogeneous Integration by Materials

Conductors

- ✓ Nanomaterials (CNT, graphene, nanowires)
- ✓ Metals (Cu, Al, W, Ag, etc.)
- ✓ Composites

Dielectrics

- ✓ Oxides
- ✓ Polymers
- ✓ Porous materials
- ✓ Composites

Semiconductors

- ✓ Elemental (Si, Ge)
- ✓ Compounds (IIIV, IIVI, tertiary)
- ✓ Polymers

Materials Parameters must be compatible with each other for processing and operation:

- ✓ Cost
- ✓ CTE differential
- ✓ Thermal conductivity
- ✓ Fracture toughness
- ✓ Modulus
- ✓ Processing temperature
- ✓ Interfacial adhesion
- ✓ Operating temperature
- ✓ Breakdown field strength

Heterogeneous Integration by Device

- ✓ Memory (DRAM, MRAM, Flash, other)
- ✓ Logic
- ✓ Sensors
- ✓ MEMS
- ✓ Mixed Signal
  - Power IC
  - Control IC
- ✓ Communications
  - RF
  - Electronic
  - Photonic
  - Plasmonic

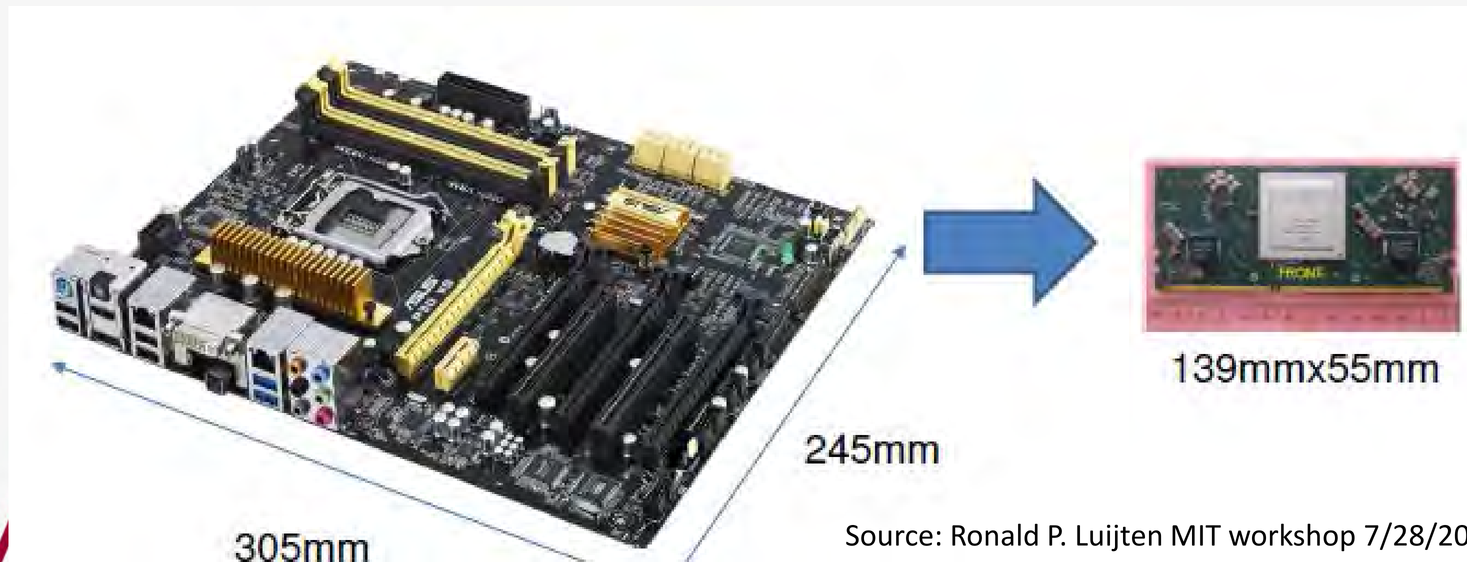
During the next 15 years many new devices will be added, each with its own packaging needs:

- ✓ Replacements for the CMOS switch
- ✓ New, more complex sensors
- ✓ New, more complex MEMS
- ✓ Synaptic processors
- ✓ Haptic devices (maybe MEMS)
- ✓ Telepathic devices
- ✓ Telekinetic devices

and devices and functions we cannot yet imagine

Rethinking Packaging For The Server

- ✓ The comparison with standard product is dramatic even with conventional PCB assembly and standard off-the-shelf components (Freescale T4240)
- ✓ Small size allows photonics to remain at rack unit edge



Source: Ronald P. Luijten MIT workshop 7/28/2015

Rethinking Packaging For The Server

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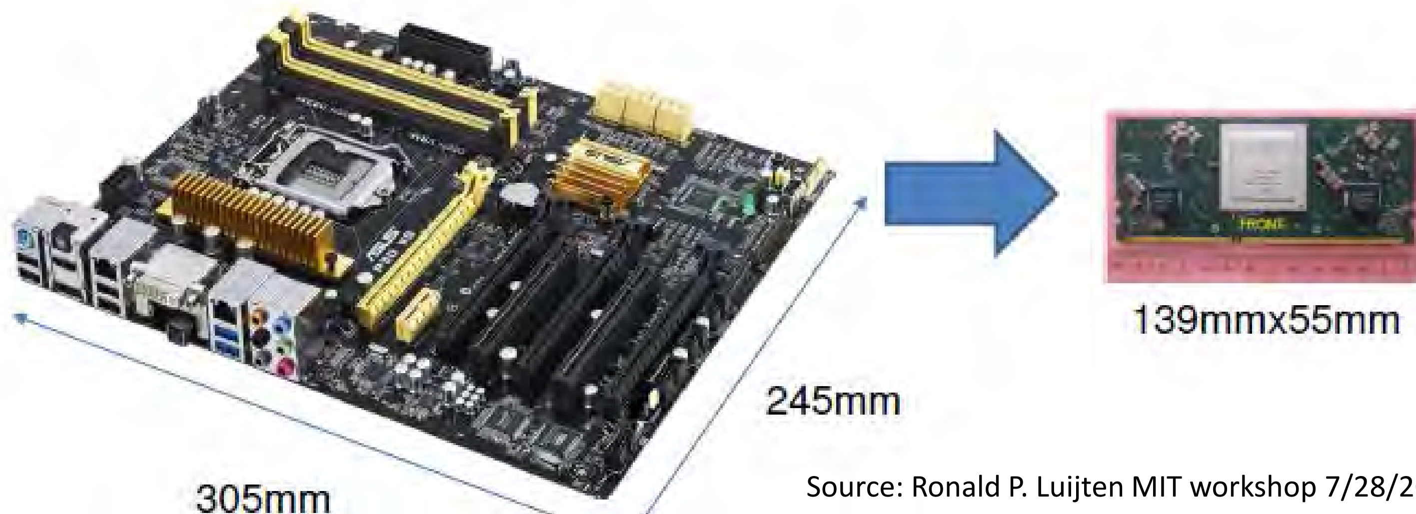
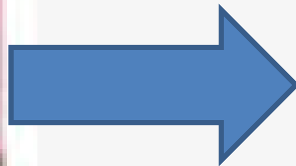
40% faster with 70% of Intel Xeon E3-1230l power yields 2X the operations per watt

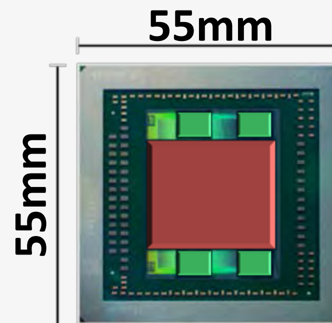


Source: Ronald P. Luijten MIT workshop 7/28/2015

What Could We Do with 3D packaging?

- ✓ 40% smaller with 16Gb high bandwidth memory
- ✓ 4096 bit memory interface
- ✓ 512GB/s memory bandwidth
- ✓ Si interposer with TSV & µbump to substrate
- ✓ Lower power
- ✓ 22 discrete die plus passive components



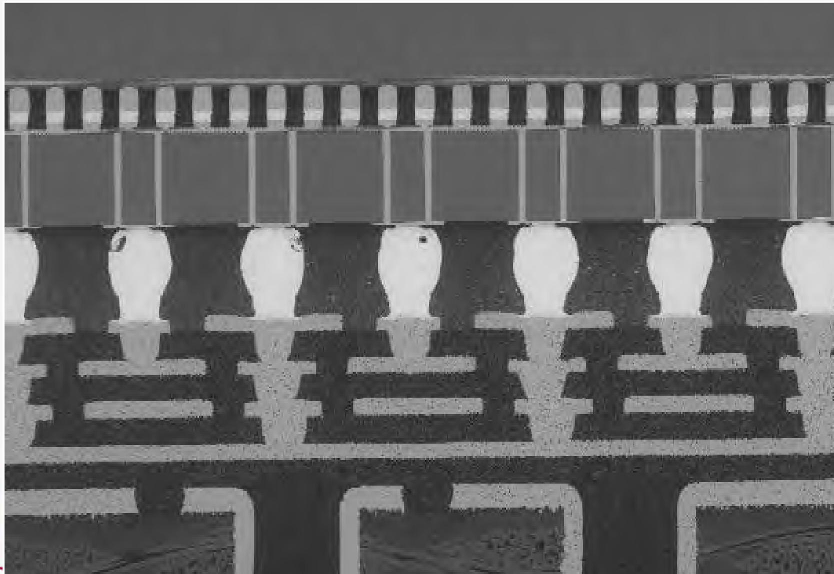


$592mm^2$ ASIC

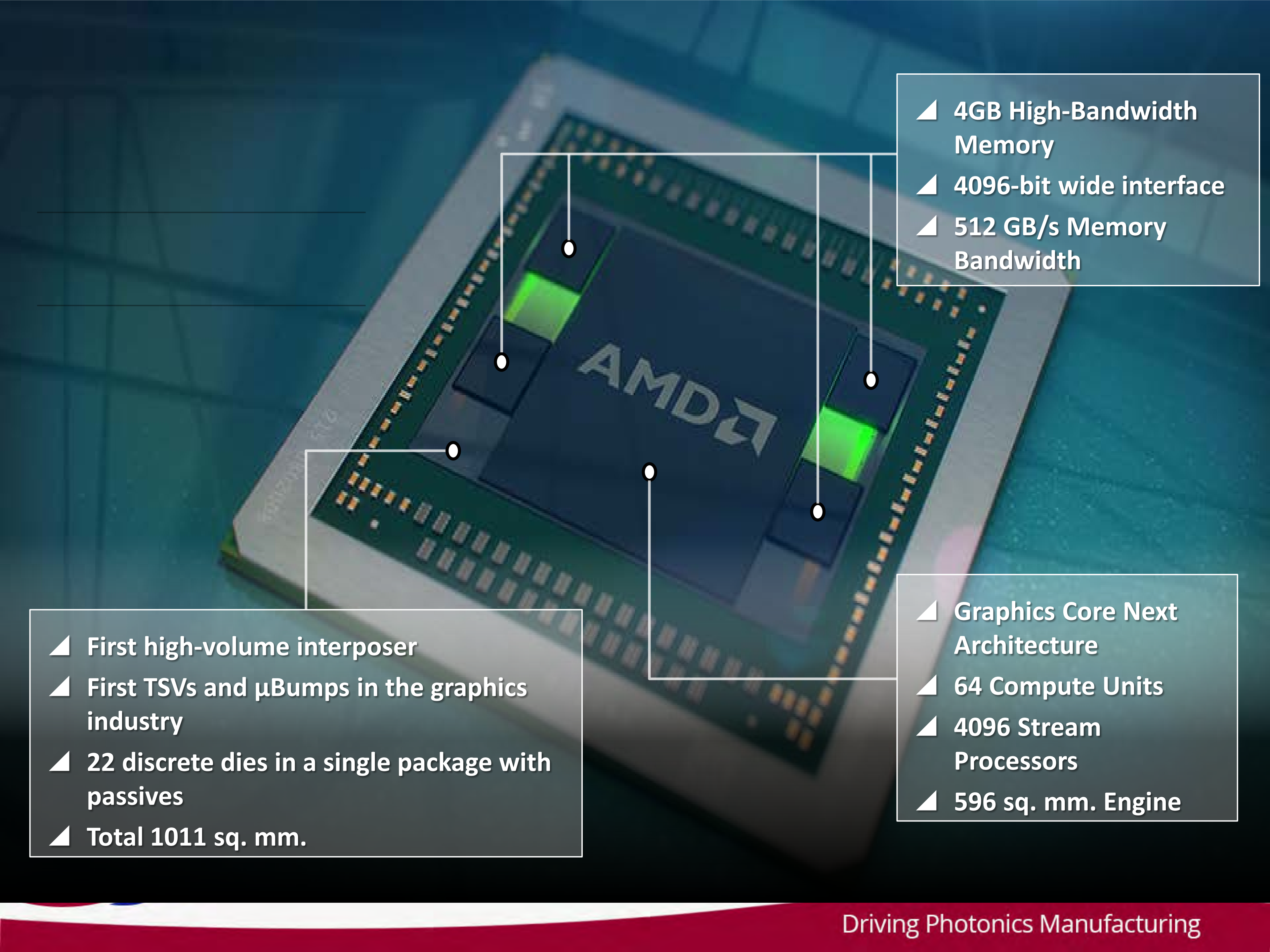
$1011mm^2$ interposer

3D Die Stacking Technology (AMD FiJI)

- ✓ Die stacking facilitating the integration of discrete dies and passives
- ✓ 8.5 years of development by AMD and its technology partners



HBM DRAM Die
HBM DRAM Die
HBM DRAM Die
HBM DRAM Die
Logic Die
GPU
Interposer
Package Substrate
TSVs
μBumps


4GB High-Bandwidth Memory
4096-bit wide interface
512 GB/s Memory Bandwidth
AMD
First high-volume interposer
First TSVs and µBumps in the graphics industry
22 discrete dies in a single package with passives
Total 1011 sq. mm.
Graphics Core Next Architecture
64 Compute Units
4096 Stream Processors
596 sq. mm. Engine

Adding Photonics To The SiP is Next

Adding a Silicon photonics chip to the stack would provide:

- ✓ Further reductions in power
- ✓ Further reductions in latency
- ✓ Decrease in total system size

This additional step in heterogeneous integration has difficult challenges in cost reducing silicon photonics and thermal management

Adding Photonics To The SiP is Next

Adding a Silicon photonics chip to the stack would provide:

- ✓ Further reductions in power

When this is our server the architecture of the data center will change

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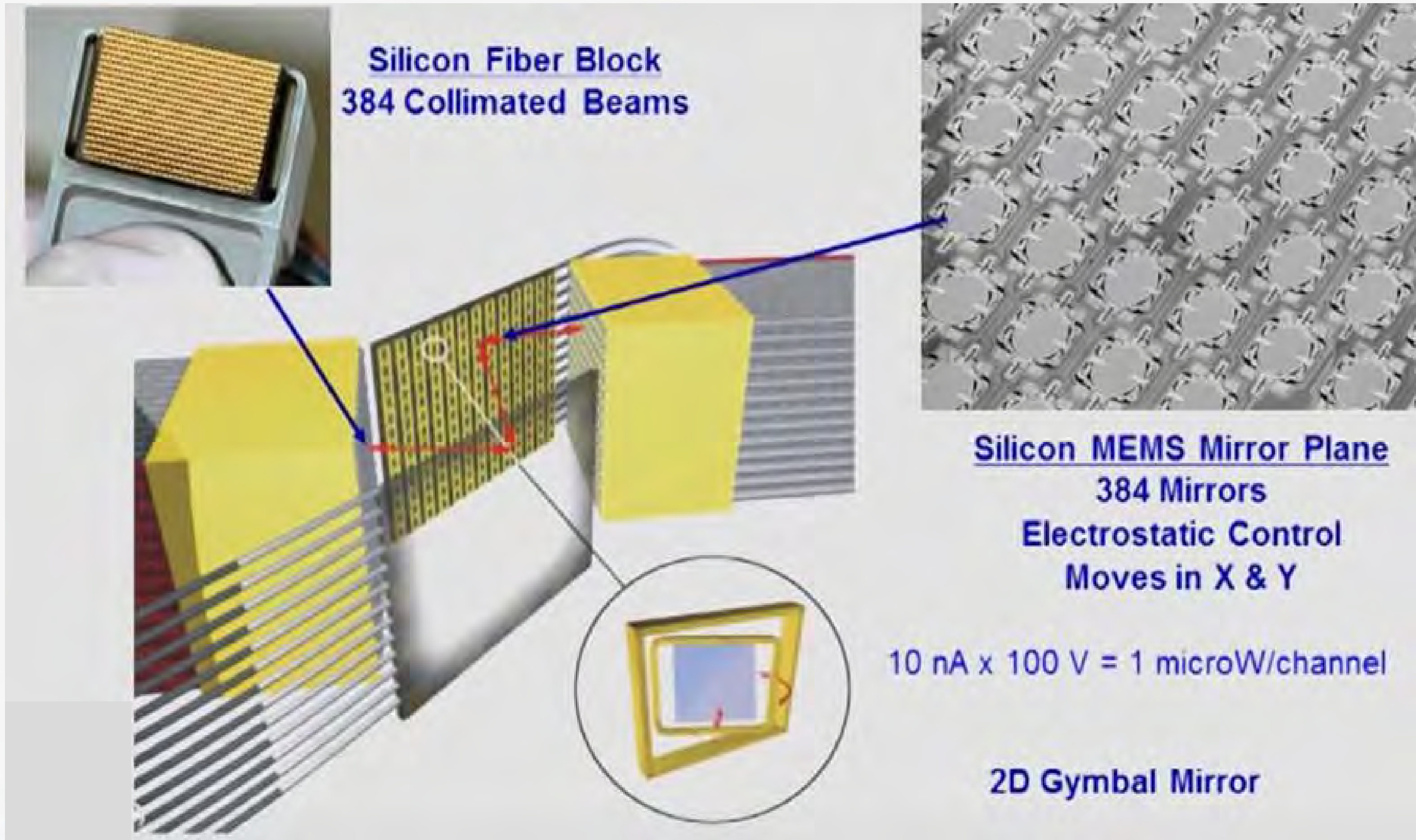
Photonic Switching Reduces Space, Latency & Power

3D MEMS Switch using mirrors



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New Packaging Materials Are Required

Carbon Conductors Look Better Than Cu

	Cu	CNT	GNR	
Max current density (A/cm^2)	**~10^6**	**> $1x10^8$**	**> $1x10^8$**	**x10^2**
Melting Point (K)	**1356**	**3800** (graphite)	**3800** (graphite)	
Tensile Strength (GPa)	**0.22**	**22.2**	**23.5**	**x10^2**
Thermal Conductivity (×10^3 W/m-K)	**0.385**	**1.75** *Hone, et al. Phys. Rev. B 1999*	**3 - 5** *Balandin, et al. Nano Let., 2008*	**x10**
Temp. Coefficient of Resistance (10^{-3} /K)	**4**	**< 1.1** *Kane, et al. Europhys. Lett.,1998*	**-1.47** *Shao et al. Appl Phys. Lett., 2008*	
Mean Free Path @ room-T (nm)	**40**	**> 1000** *McEuen, et al. Trans. Nano., 2002*	**~ 1000** *Bolotin, et al. Phys. Rev. Let. 2008*	**x25**

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Many questions still to be answered before graphene or CNT can be considered as practical interconnect materials. The results so far are very promising.

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Conductors Are Changing

Composite Copper is in evaluation.

Current status:

Measurement	Conventional Copper	TeraCopper®
Resistivity (Ohm·cm)	1.66×10^{-6}	1.26×10^{-6}
Conductivity (S/m)	6.02×10^{7}	7.94×10^{7}
Increase in Conductivity	N/A	32%
Avg. Current Capacity(Amps/cm²)	3.88×10^{4}	5.57×10^{4}
Increase in Current Capacity	N/A	44%

The first electrical performance improvement in copper since 1913 makes composite copper the most electrically conducting material known at room temperature.

Targets for improvement compared to conventional copper are:

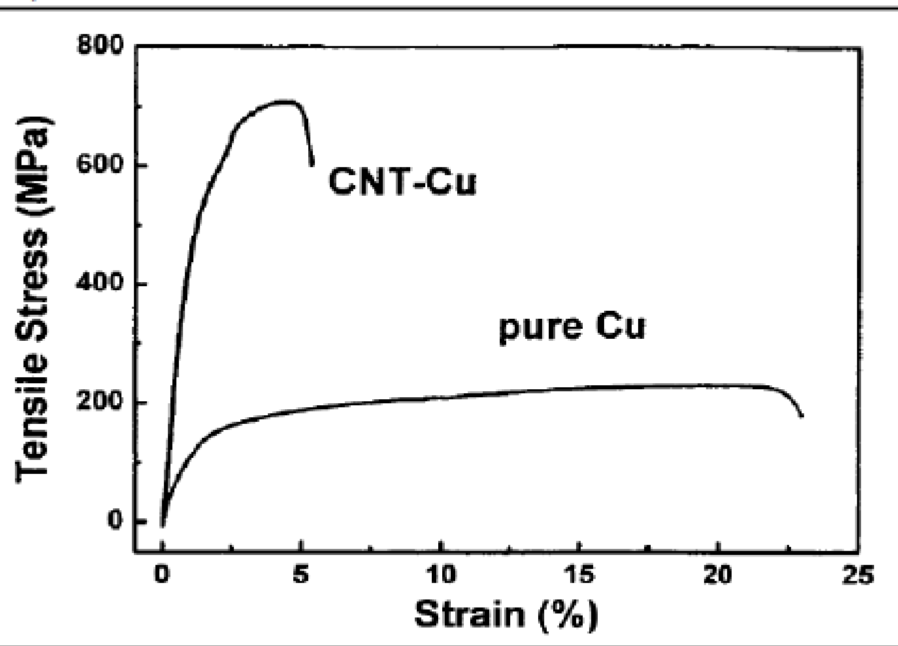
- ✓ **100 % increase in electrical conductivity**
- ✓ **100% increase in thermal conductivity**
- ✓ **300% increase in tensile strength**

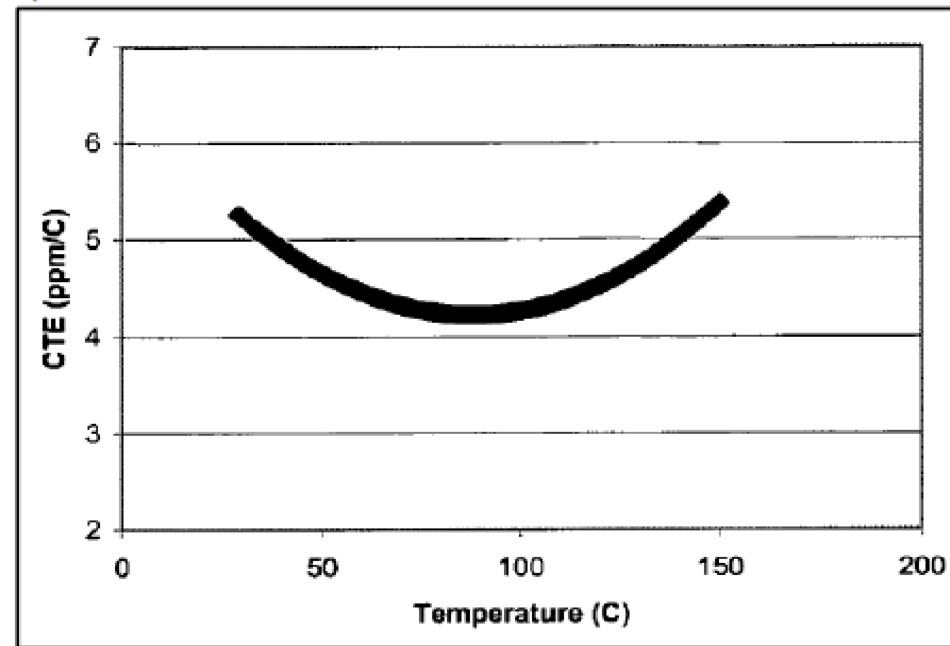
Source: NanoRidge

Composite Cu Properties

Measured Properties show:

- ✓ The strength of the Cu-SWCNT composite is more than twice that of pure copper
- ✓ Ductility is significantly lower.
- ✓ Coefficient of thermal expansion ranges between 4 to 5.5x10-6/°C vs 17x10-6/°C for pure Cu.





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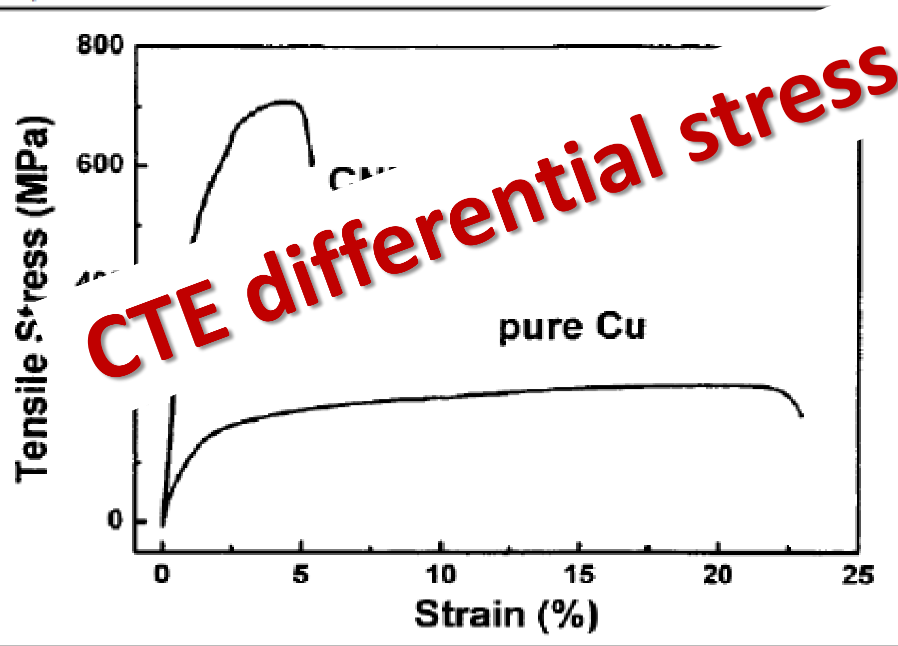
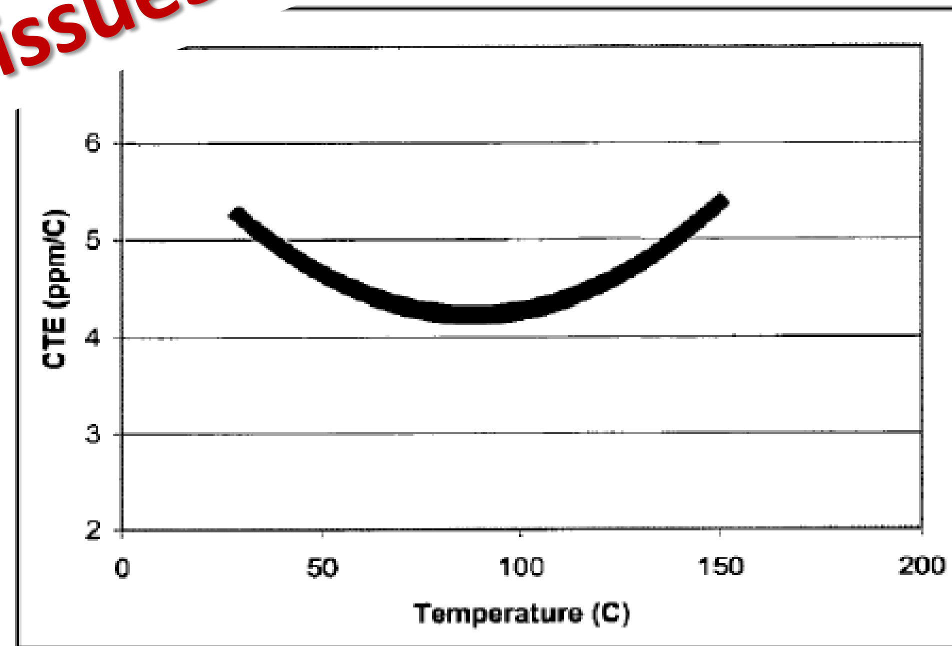
- ✓ Coefficient of thermal expansion ran... ...4 to 5.5x10-6/°C vs 17x10-6/°C fo...

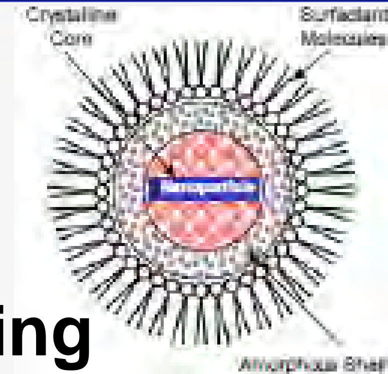
CTE differential stress issues should be solved!

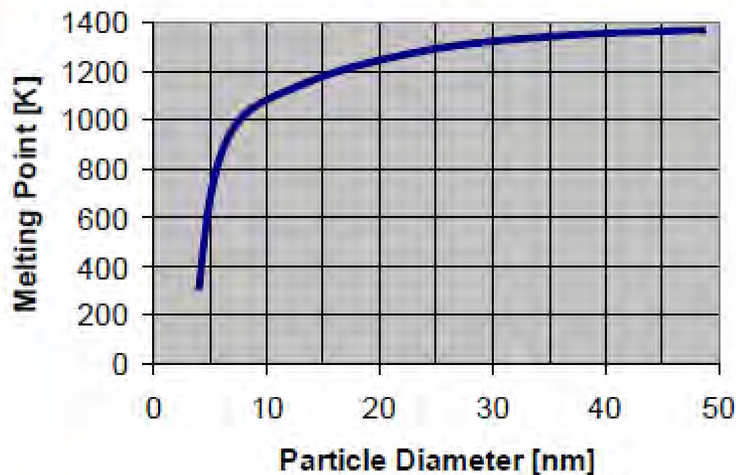


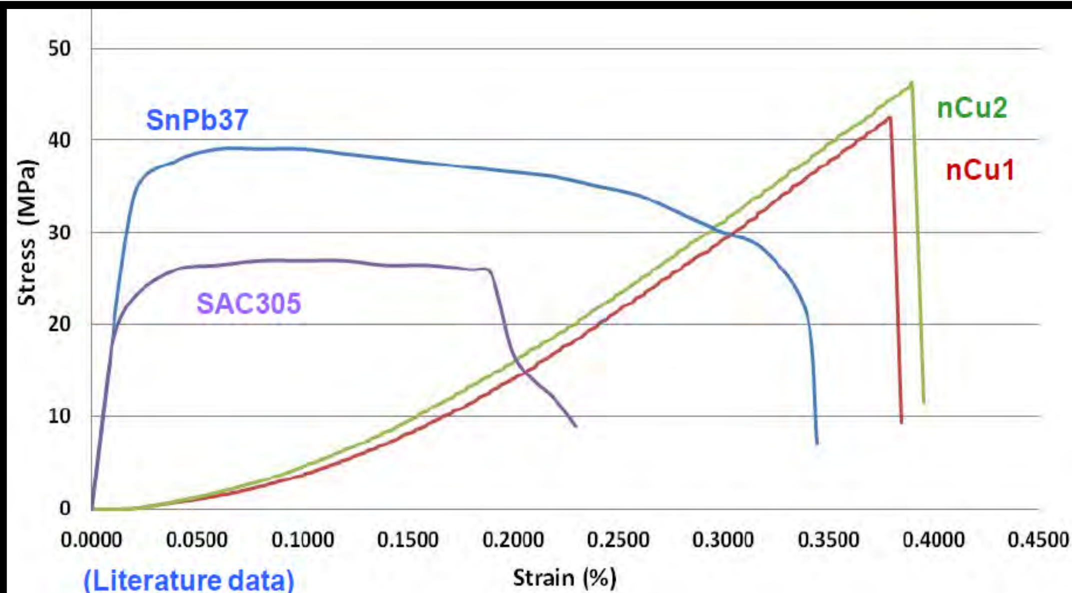


Low temp Cu Nano-solder

- ✓ **Package assembly at low temp (100C)**
- ✓ **Reflow solder to PCB <200C**
- ✓ **Consistent with Direct Interconnect Bonding**
- ✓ **Thermal/electrical conductivity 10-15X that of SAC**







All Processing At “Use Case” Temperature And Matched CTE

- ✓ Warpage problem is resolved
- ✓ No stress built in due to bonding/soldering at high temperature well above “use case”
- ✓ Limited stress induced due to differential CTE

The materials and processes needed have been demonstrated but not yet integrated

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Photonic Systems Manufacturing Consortium

Photonics and the Internet of Things

Driving Photonics Manufacturing

Packaging For The Internet Of Things

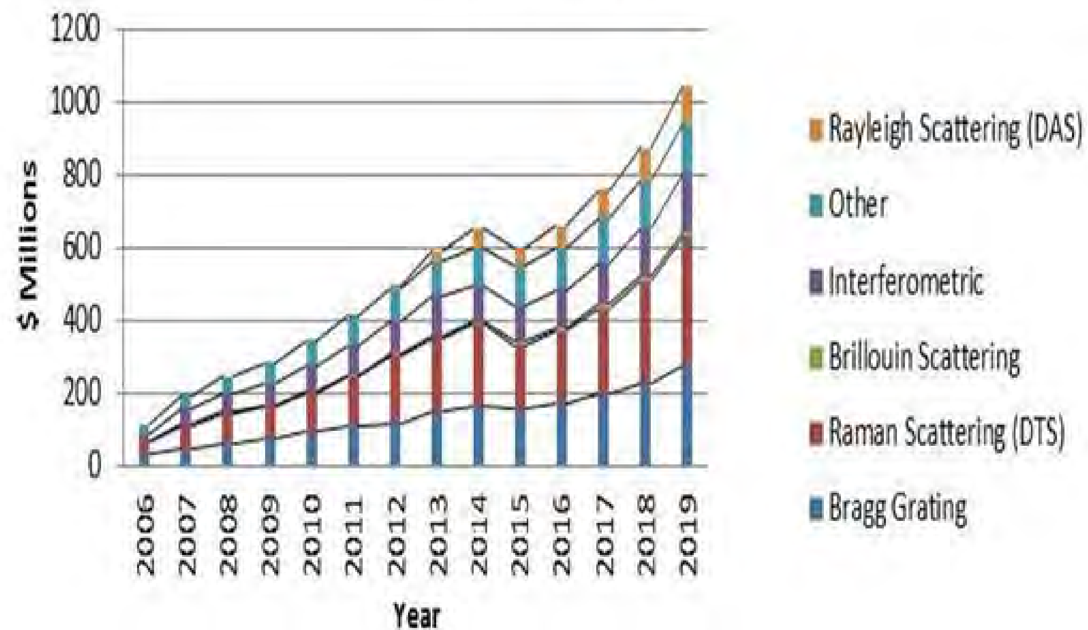
IoT packaging will require heterogeneous integration of sensors, RF components, memory, logic and photonics for environments not well controlled:

- ✓ No latency requirements
- ✓ Do nothing well
- ✓ Maintenance free
- ✓ Self powered (energy scavenging-photovoltaics)

Photonic Sensors Will Be IoT Components
With unique packaging requirements

Fiber optic sensors are an enabling technology in emerging applications in harsh environments

- ✓ Military applications
- ✓ Oil and gas industry
  - Exploration to drilling
  - Completion
  - Production
  - Reservoir management



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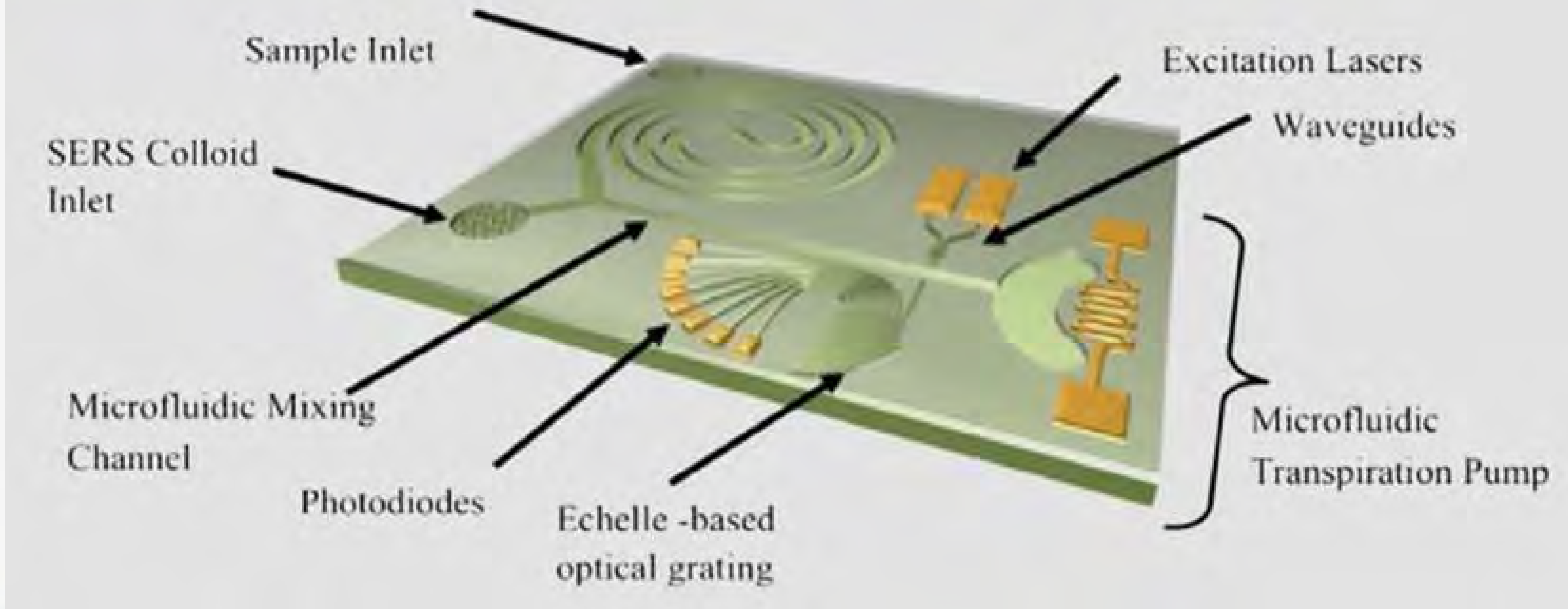
MEMS/Photonic Gas Sensors For The IoT

Silicon-based Raman Spectrometer on a chip



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Packaging Innovation For IoT

The packaging of sensors with RF and control electronics integrated into a reliable IoT hub poses difficult challenges for commercial IoT photonic/electronic products

Reducing Power And Latency While Increasing Performance And Reducing Size And Cost

How Can We Reduce Power?

- ✓ Continue Moore's Law Scaling
- ✓ Reduce leakage currents
  - Transistors are less than 10% of IC power today and going down

(**new transistor designs**)

- ✓ Reduce on-chip Interconnect power by:
  - Improved conductor conductivity (**new material**)
  - Decrease capacitance (**new material**)
- ✓ Reduce interconnect length (**3D integration**)
- ✓ Reduce operating frequency
- ✓ Reduce operating voltage
  - Voltage regulator per core

(**increased parallelism**)

- ✓ Reduce high speed electrical signal length
  - Move photons closer to the transistors (**On-package photonics**)

Potential Power Solutions Beyond Core Packaging Technologies

- ✓ Distribute power to the PCB/package at 200V and use it in integrated circuits at low voltage I^2R
- ✓ Drop operating voltage as low as possible (dynamically) CV^2
- ✓ Drop operating frequency (dynamically) CV^2
- ✓ Move photonics as close to the transistors as possible
- ✓ Increase conductivity with new materials I^2R
- ✓ Move components as close together as possible (use the 3rd dimension) I^2R
- ✓ Decouple inductance with local high k dielectrics
- ✓ Use ULK k dielectrics for isolation CV^2
- ✓ Turn off System power not needed for short periods (sub-microsecond?)

Potential Power Solutions Beyond Core Packaging Technologies

- ✓ Distribute power to the PCB/package at 200V and use it in integrated circuits at low voltage **I^2R**
- ✓ Drop operating voltage as low as possible (dynamically) **CV^2**

The combined impact of the changes discussed can provide a power reduction of 10^3; we have 15 years to implement these technologies and find another order of magnitude to reach 10^4

- ✓ Use ULK k dielectrics for isolation **CV^2**
- ✓ Turn off System power not needed for short periods (sub-microsecond?)

We Have A Growing Inventory Of SiP Components

Difficult Challenges remain with integration of these components into a cost effective, functional SiP that meets the performance, power and latency requirements

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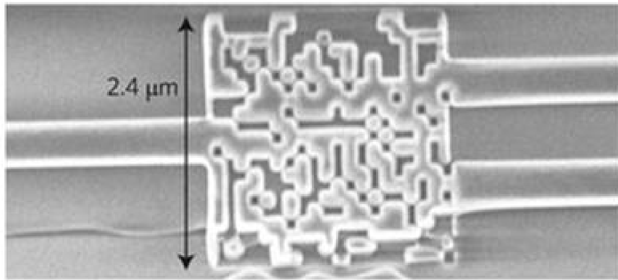
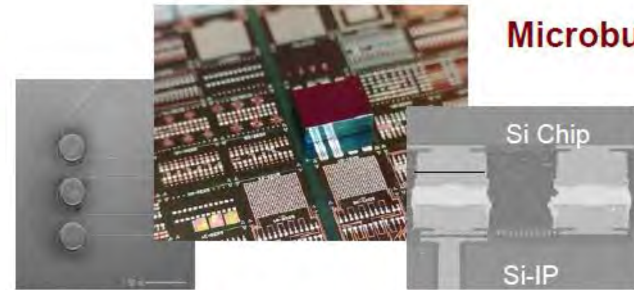
The Building Blocks For Integrating Photonics into SiP

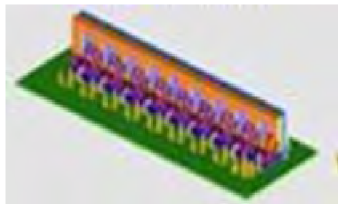


Beam splitters

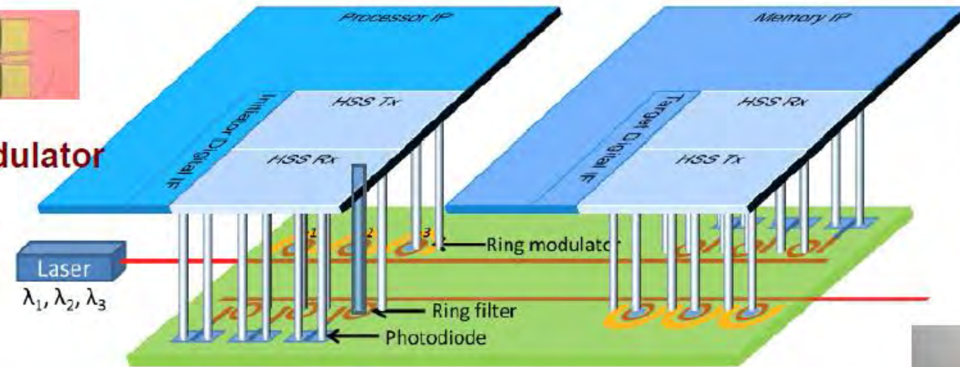


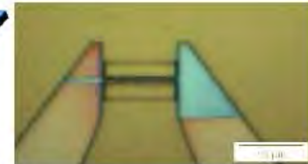
Microbumps

Optical modulator

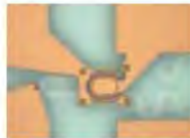


Optical bus





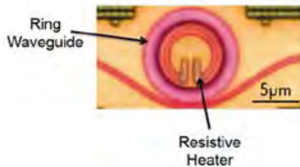
Photodetector

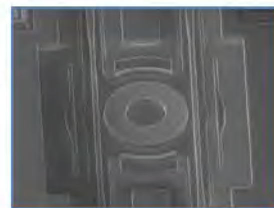


Laser source

Fiber coupler

Active Wavelength Locking





Ring modulator

Waveguides

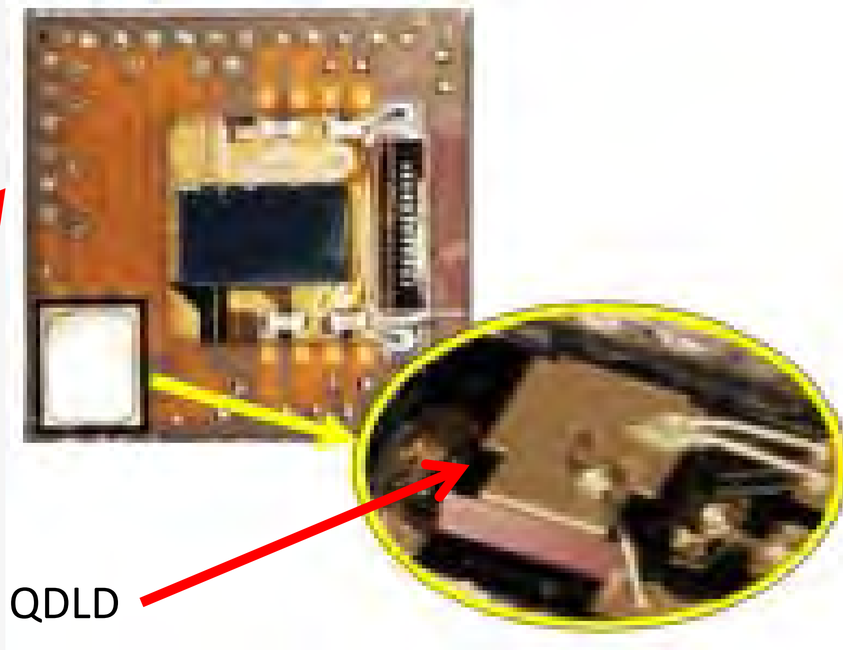
WDM filters

Source: ECTC2014 - Stephane BERNABE

Si Photonics Transceiver With Quantum Dot Laser

- ✓ Good Temperature stability of output power
- ✓ Petra projects BW density of 400Gbps/mm with photonic/electronic in SiP
- ✓ Photonic/Electronic chip 5mmx5mm
- ✓ Uses TGV
- ✓ 5mW/Gbps

Integration approach of the Photonic Electronic Technology Research Association (***Petra***)



QDLD

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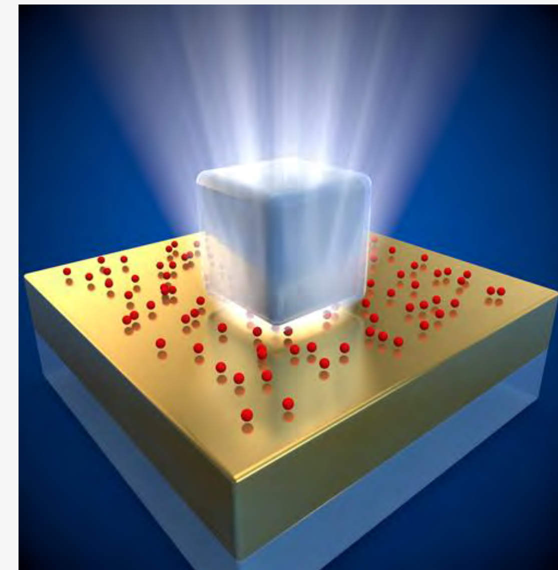
New Active Components Are Appearing

Ultrafast emission source using plasmonic nano-antennas(NPAs) has been fabricated and characterized

- ✓ A promising alternative to on-chip lasers
- ✓ NPA Coupled with quantum dots
- ✓ Radiative quantum efficiency over 50%
- ✓ <11 pico-seconds emission rise time
- ✓ Emission rate >90GHz

Artists rendering of nanopatch plasmonic antenna (NPA, silver cube) mounted on Au substrate (gold) separated by a polymer containing colloidal quantum dots (QD, red).



(Source: Duke University)

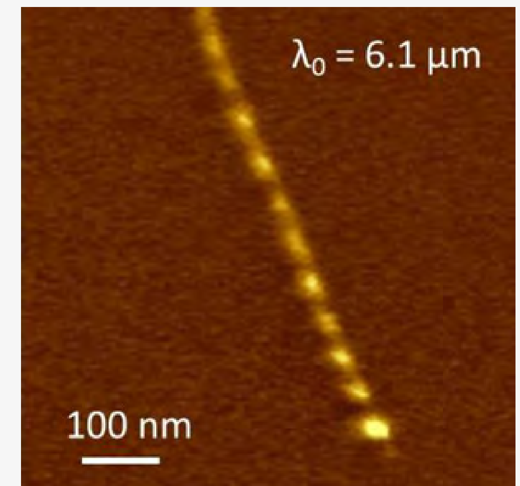
Sub-wavelength Confinement of Photon Energy

Source: Lawrence Berkeley National Laboratory

Recent development has generated and detected plasmons with the strongest confinement factors ever:

- ✓ Confinement 100M x smaller than free space plasmon wavelength
- ✓ Plasmon is ~100 X smaller than the photon wavelength
- ✓ Confinement in a single wall carbon nanotube ~1ηm diameter

Image taken at Berkeley National Laboratory of Plasmons confined in a Carbon Nanotube using a scattering-type scanning near-field optical microscopy (s-SNOM)



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Source: Lawrence Berkeley National Laboratory

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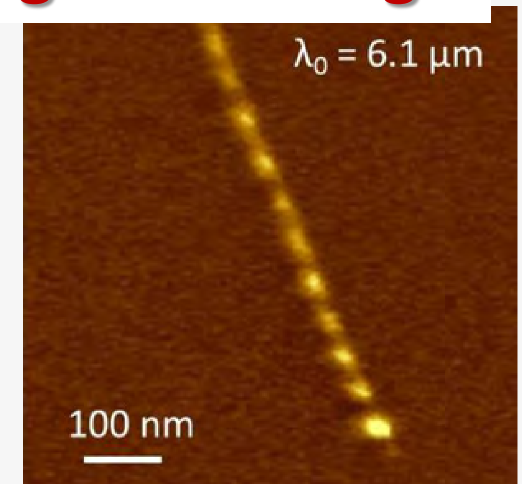
- ✓ Plasmon is ~100 X smaller than the photon wavelength

There are many interactions between photons, plasmons and electrons under investigation for use in O-to-E and E-to-O conversion among other things

Image taken at Berkeley National Laboratory of Plasmons confined in a Carbon Nanotube using a scattering-type scanning near-field optical microscopy (s-SNOM)



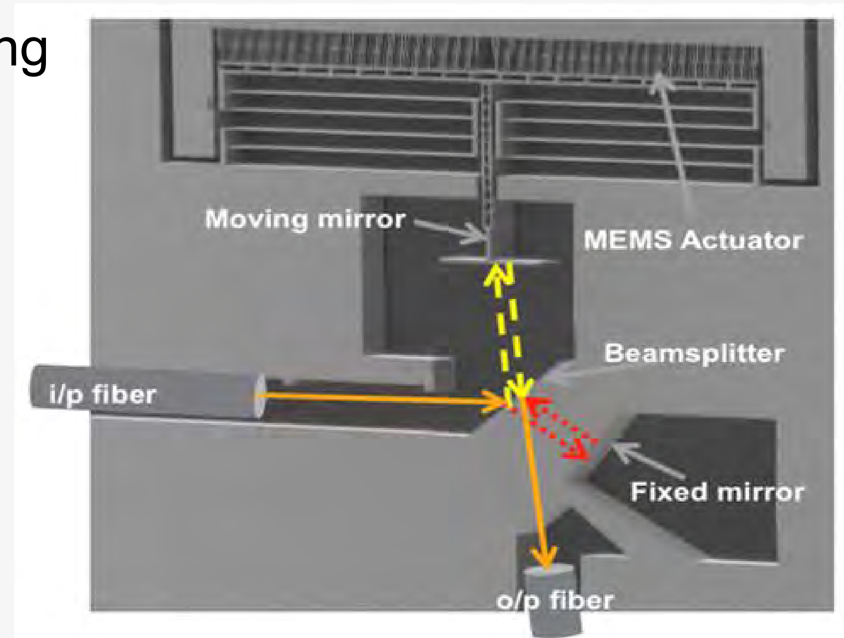
Source: Lawrence Berkeley National Laboratory

MEMS Photonic Products Are On The Market

A Photonic MEMS spectrometer is available

- ✓ Portable low power
- ✓ Low cost ($2K today Vs $10k for bench top of similar performance)
- ✓ Projected $500 high volume price
- ✓ Wearable wrist band products coming

Source: Si-Ware



MEMS Photonic Spectrometer combines all functions of today's bench mounted systems

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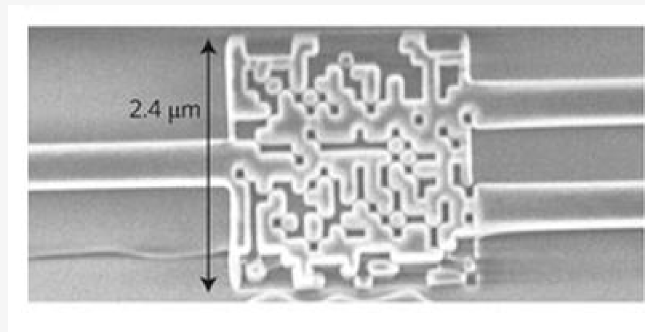
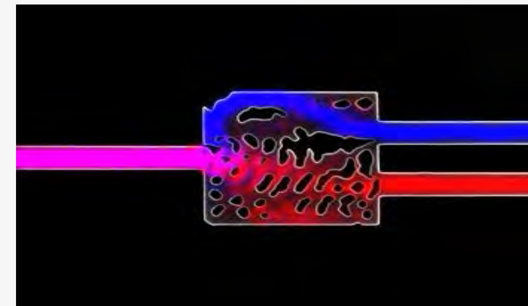
New Passive Components Are Appearing

One objective is to replace on chip electrical interconnect with photons and these passive components are a step in that direction.



Beam Splitter 2.4µm x 2.4µm size
Made with standard CMOS process
Less heat, lower cost, 1700X smaller
Source: University of Utah



Beam Splitter
Made with standard CMOS process
Less heat, lower cost, >1700X smaller
Source: Stanford University

New Passive Components Are Appearing

One objective is to replace on chip electrical interconnect with photons and these passive components are a step in that direction.

There will be many new devices not yet proven and some not yet invented that will be components in electronic/photonic 3D-SiP packaging during the life of this roadmap

Beam Splitter 2.4µm x 2.4µm size
Made with standard CMOS process
Less heat, lower cost, 1700X smaller
Source: University of Utah

Beam Splitter
Made with standard CMOS process
Less heat, lower cost, >1700X smaller
Source: Stanford University

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KEY Attributes Of Photonic Packaging

- ✓ Heterogeneous integration for diverse materials (different CTE, electrical, optical, mechanical properties)
- ✓ Physical size
- ✓ Hermeticity
- ✓ Co-Design and simulation tools for all components: passive, RF, photonic, electronic, plasmonic, MEMS
- ✓ Physical density of components
- ✓ 3D integration in the package
- ✓ Cross talk
- ✓ Incorporate changes over life of the roadmap in components and materials available
- ✓ Models for new composite materials
- ✓ Thermal management
- ✓ Stress management
- ✓ Electrical resistance/inductance/capacitance
- ✓ Environmental compatibility
- ✓ Component attach for different materials and component types
- ✓ Reliable power delivery with near threshold operation
- ✓ Reliability under stresses of the use case (thermal, mechanical shock, electrical, chemical)
- ✓ Photons into and out of the package
- ✓ Electrical connection into and out of the package
- ✓ Yield
- ✓ Warpage (thinned components, package substrate)
- ✓ Test for complex SiP electronic-photonic products
- ✓ High volume/parallel manufacturing processes
- ✓ Low temperature assembly processes

How Do We Test SiP Electronic-Photonic products ?

- ✓ **Integrate Optical Ports to Provide Access to Test Optical Functions**
  - Optical Sources to Generate Test Light Beam
    - Multiple Beams
    - Wavelength
    - Power Level
    - Modulation Method
    - Polarization
  - Suitable Detectors required
    - Multiple Detectors
    - Wavelength
    - Sensitivity
    - Bandwidth
    - Skew Detection
  - Coupling Methods
    - From/To Fiber/Fibers
    - From/To Waveguide/Waveguides
    - From/To “Free Space”
- ✓ **Mix with Electronic Test Points**

How Do We Test SiP Electronic-Photonic products ?

- ✓ **Integrate Optical Ports to Provide Access to Test Optical Functions**
  - – Optical Sources to Generate Test Light Beam
    - Multiple Beams
    - Wavelength

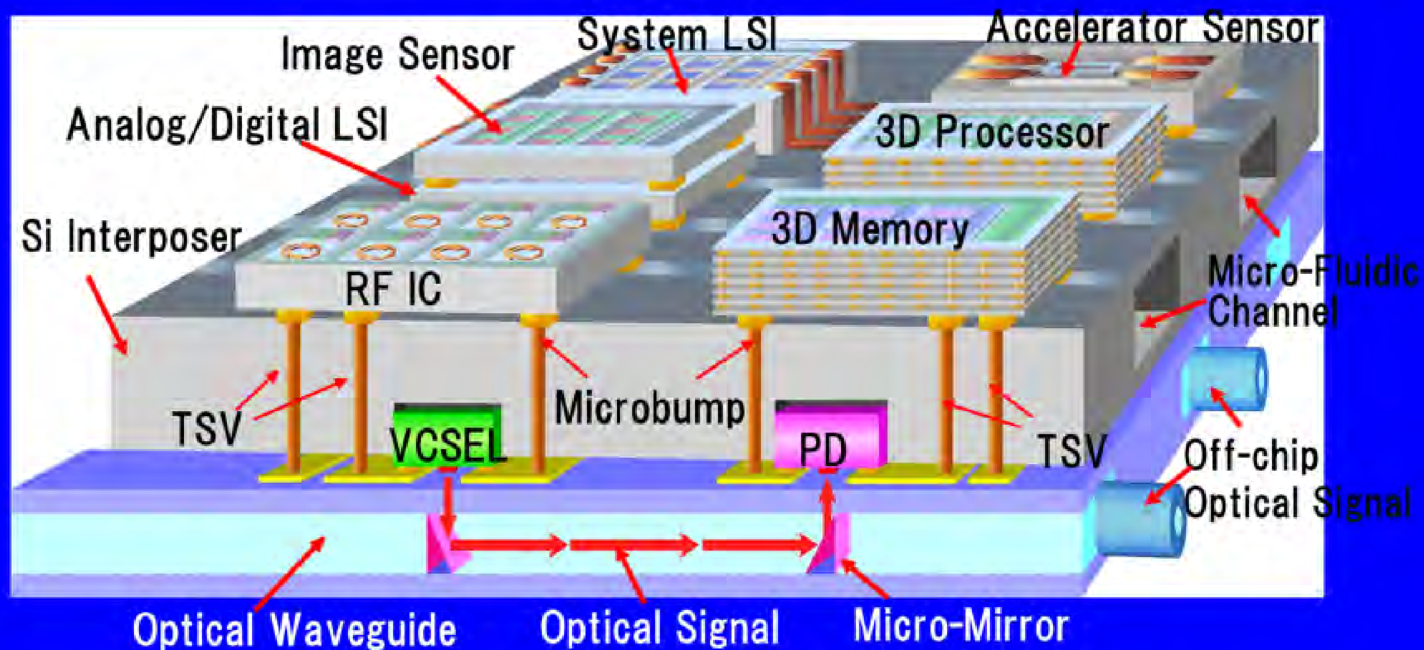
These Issues will be addressed in the Assembly and Test TWG Webinar November 17th but access must be part of package design and test engines must be incorporated into the package

- From/To Fiber/Fibers
- From/To Waveguide/Waveguides
- From/To "Free Space"

- ✓ **Mix with Electronic Test Points**

3D-SiP Heterogeneous Integration Concept

This may be the HI package of the future

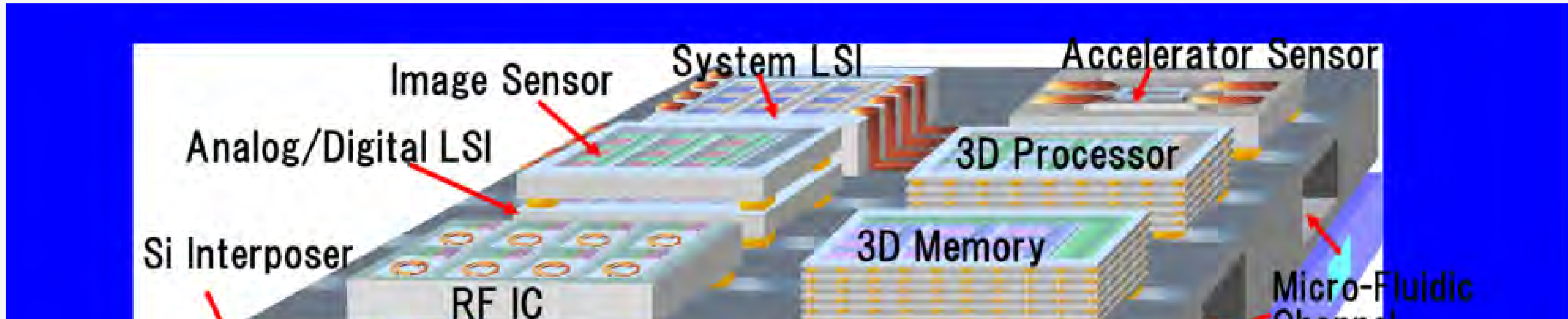


- *MEMS sensors for high sensitive sensing of moving elements*
- *Image sensor for high performance imaging processing*
- *3D processor, 3D memory for high performance data computing*
- *Optical interconnection for high speed data transmission*
- *Micro-fluidic channels for heat sinking*

K.W. Lee et al., IEDM, 2009

3D-SiP Heterogeneous Integration Concept

This may be the HI package of the future



The individual components exist but cannot yet be cost effectively integrated at package level

- *MEMS sensors for high sensitive sensing of moving elements*
- *Image sensor for high performance imaging processing*
- *3D processor, 3D memory for high performance data computing*
- *Optical interconnection for high speed data transmission*
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K.W. Lee et al., IEDM, 2009

Summary

Requirements for Photonics Packaging will be driven by IoT and the Global Network and its components and Subsystems. 15 year requirements are:

- ✓ Cost and power reduced by $>10^4$
- ✓ Flatten the architecture, increase ports by $>10^6$
- ✓ Reduced latency
- ✓ Support software defined networks
- ✓ Photonics to the package

A majority of improvement will come from Heterogeneous Integration and 3D-SiPh packaging.

Innovation in architecture, materials and processes are essential satisfy the Roadmap Requirements.

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Thank You for Your Attention

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Driving Photonics Manufacturing